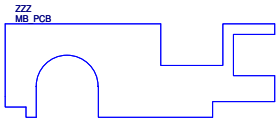


MODEL NAME : VAZ90
PCB NO : LA-A161P
BOM P/N :
revision: A00



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Schematic Document

Jarama (Haswell Y-series)

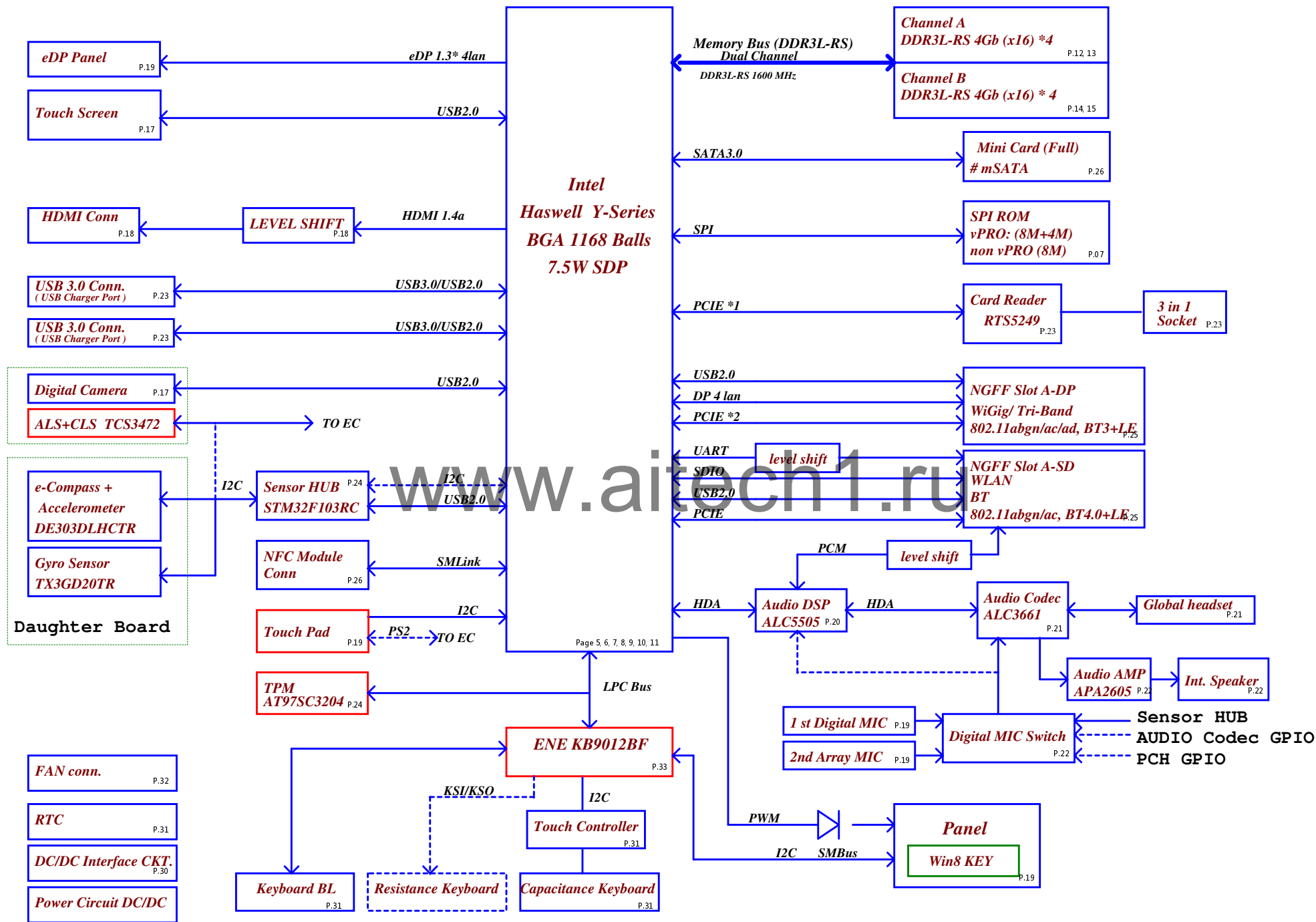
www.waitech1.ru

- @ : Nopop Component
- CONN@ : Connector Component
- vPRO@ : SPI ROM (8M+4M) Component
- nvPRO@ : SPI ROM (8M) Component
- CS@ : Connected Standby Component
- Non-CS@ : Non-Connected Standby Component

2013-08-14

Rev: A00

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		LA-A161P			X02
Date: Wednesday, August 14, 2013		Sheet 1 of 49			



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Project Code : VAZ90

File Name :

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				Rev	A00

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0				
1	12K +/- 1%				
2	15K +/- 1%				
3	20K +/- 1%				
4	27K +/- 1%				
5	33K +/- 1%				
6	43K +/- 1%				
7	56K +/- 1%				
8	75K +/- 1%				
9	100K +/- 1%				
10	130K +/- 1%				
11	160K +/- 1%				
12	200K +/- 1%				
13	240K +/- 1%				
14	270K +/- 1%				
15	330K +/- 1%				
16	430K +/- 1%				
17	560K +/- 1%				
18	750K +/- 1%				
19	NC				

BOARD ID Table

Board ID	PCB Revision
0	Non- VPRO 0.1 (SSI)
1	VPRO 0.2 (PT)
2	VPRO 0.3 (ST)
3	VPRO 1.0 (XB)
4	
5	
6	
7	
8	
9	
10	VPRO 0.1 (SSI)
11	Non- VPRO 0.2 (PT)
12	Non- VPRO 0.3 (ST)
13	Non- VPRO 1.0 (XB)
14	
15	
16	
17	
18	
19	

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	External USB3
	1	External USB3
	2	NGFF CARD WLAN
	3	Touch Panel
	4	Camera
	5	Sensors HUB
	6	NGFF(WiGig)
	7	

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	NGFF(WiGig)
	2	HDMI

SMBUS Control Table


	SOURCE	NGFF	BATT	Charger	NFC	XDP	ALS	Panel T-COM	Keyboard
EC_SMB_CK1 EC_SMB_DA1	KB9012		V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012						V		V
EC_SMB_CK4 EC_SMB_DA4	KB9012						V		
PCH_SML0CLK PCH_SML0DATA	PCH				V				
PCH_SML1CLK PCH_SML1DATA	PCH								
PCH_SMBCLK PCH_SMBDATA	PCH					V			
CL_CLK CL_DATA	PCH	V							


CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	WiGig	CLKOUT_LPC_0	TPM , EC LPC
	CLKOUT_PCIE1	Card Reader	CLKOUT_LPC_1	LPC Debug
	CLKOUT_PCIE2	NGFF CARD WLAN		
	CLKOUT_PCIE3	WiGig		
	CLKOUT_PCIE4			
	CLKOUT_PCIE5			

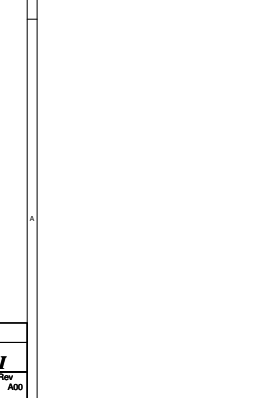
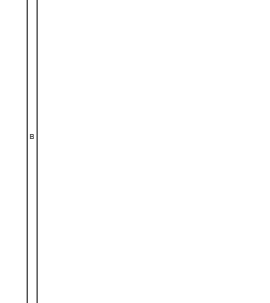
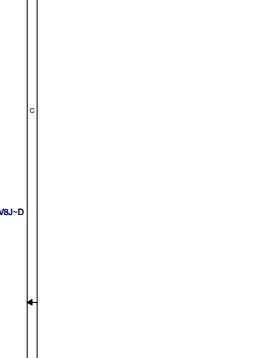
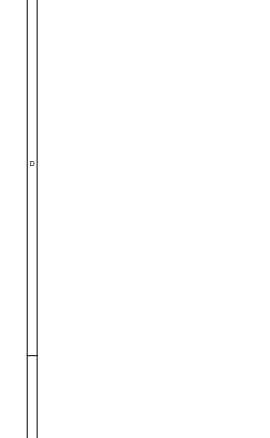
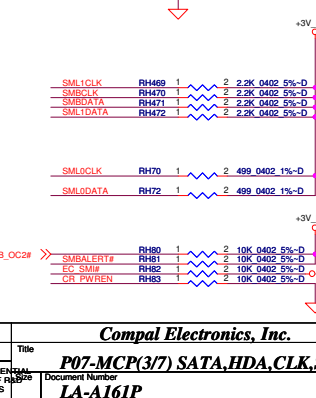
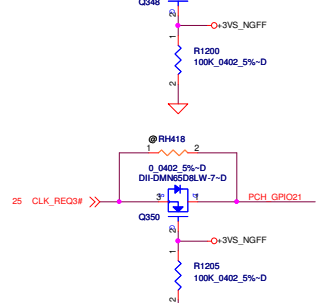
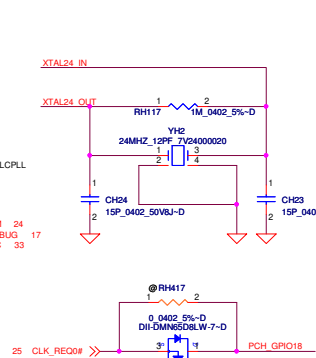
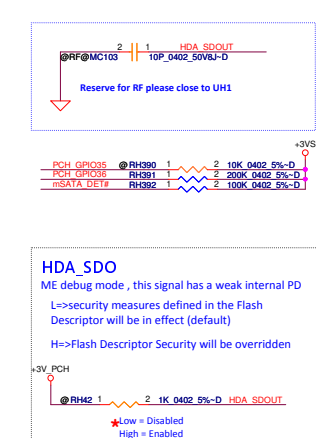
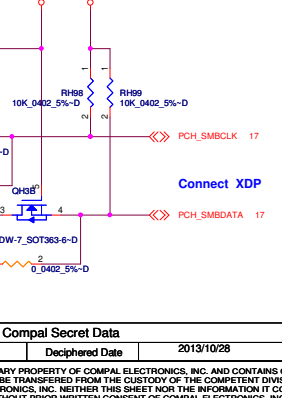
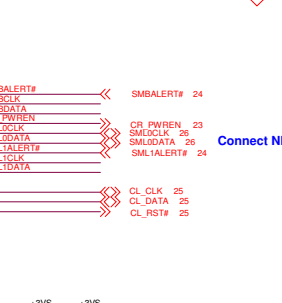
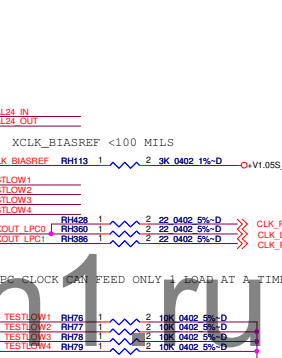
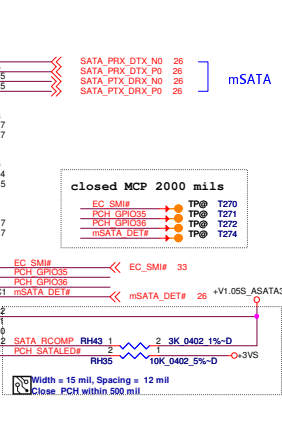
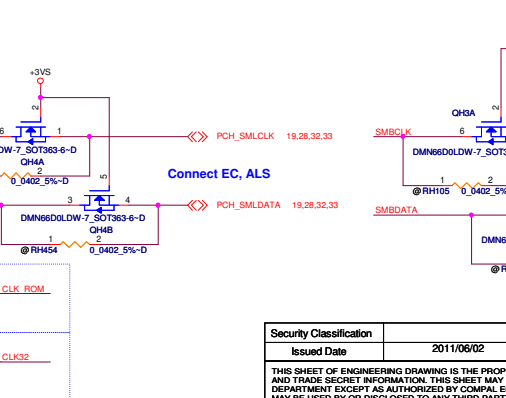
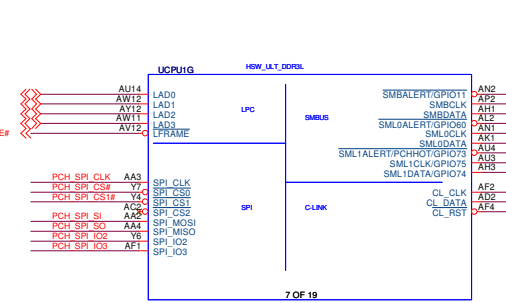
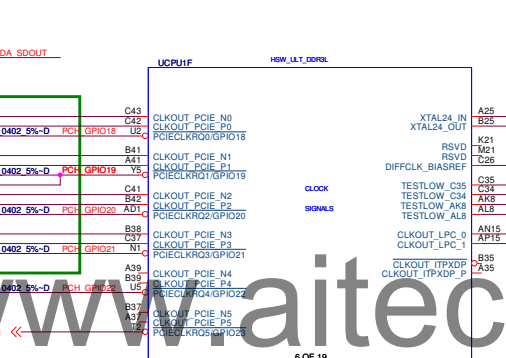
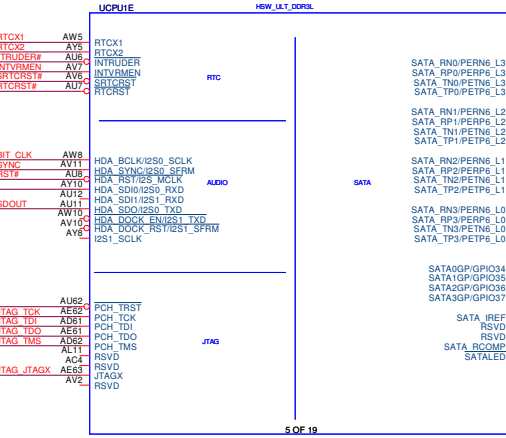
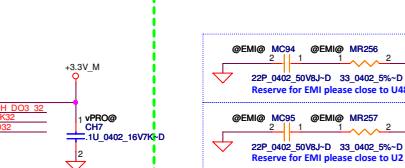
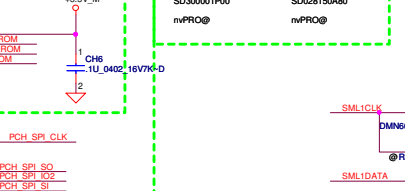
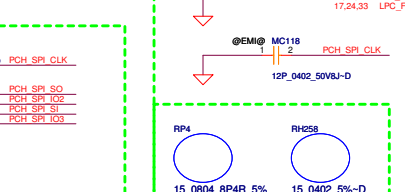
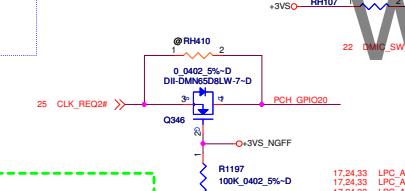
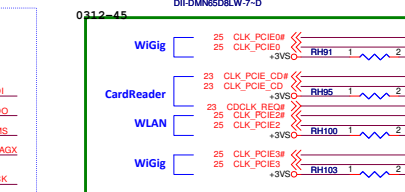
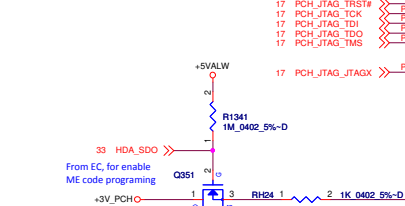
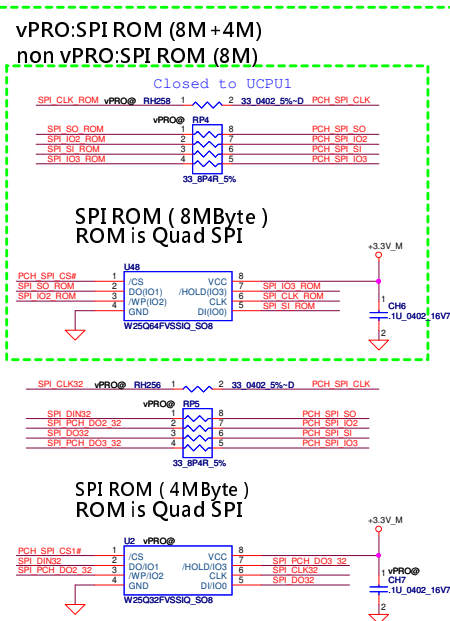
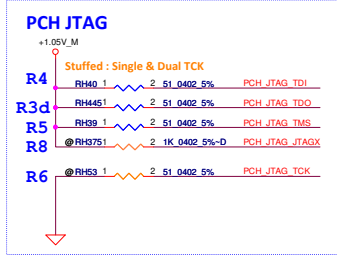
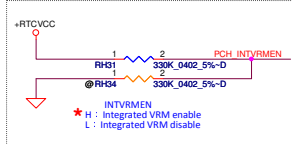
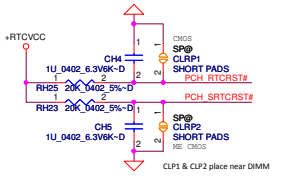
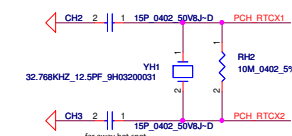
SATA	DESTINATION
SATA0	m-SATA
SATA1	
SATA2	
SATA3	

PCI EXPRESS	DESTINATION
Lane 1	NGFF(WiGig)
Lane 2	CardReader
Lane 3	NGFF(WLAN)
Lane 4	NGFF(WiGig)
Lane 5	
Lane 6	

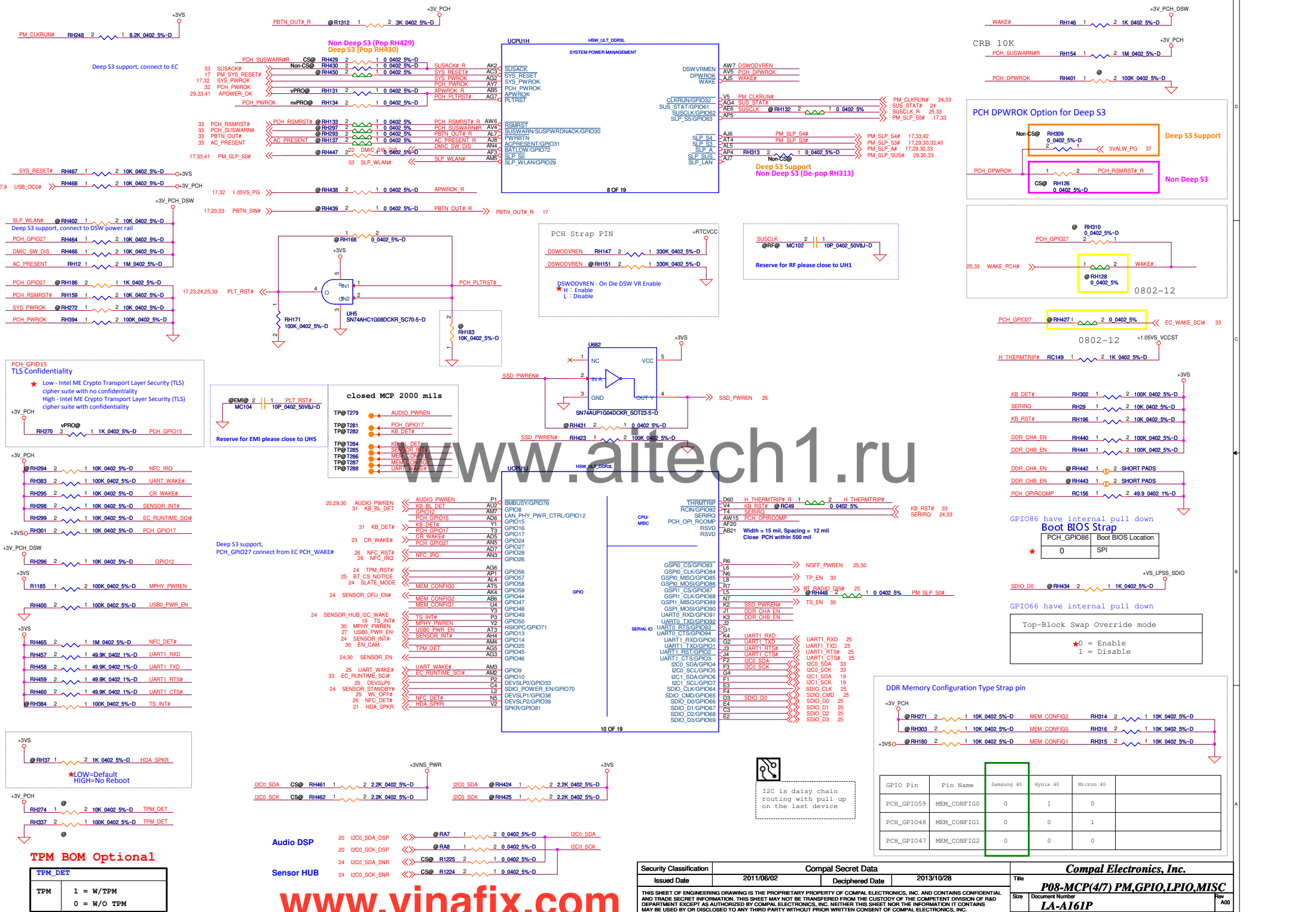
Symbol Note :

 : means Digital Ground

 : means Analog Ground



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2011/06/02	
2011/06/02		2013/10/28		P07-MCP(3/7) SATA,HDA,CLK,SPI	
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Date		Wednesday, August 14, 2013		Sheet 7 of 49	

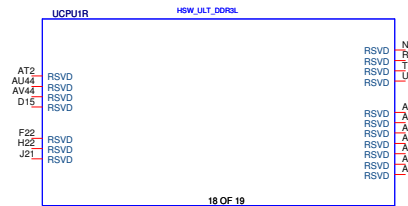
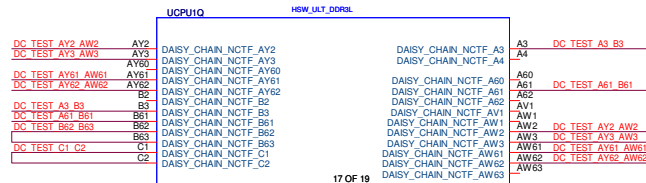
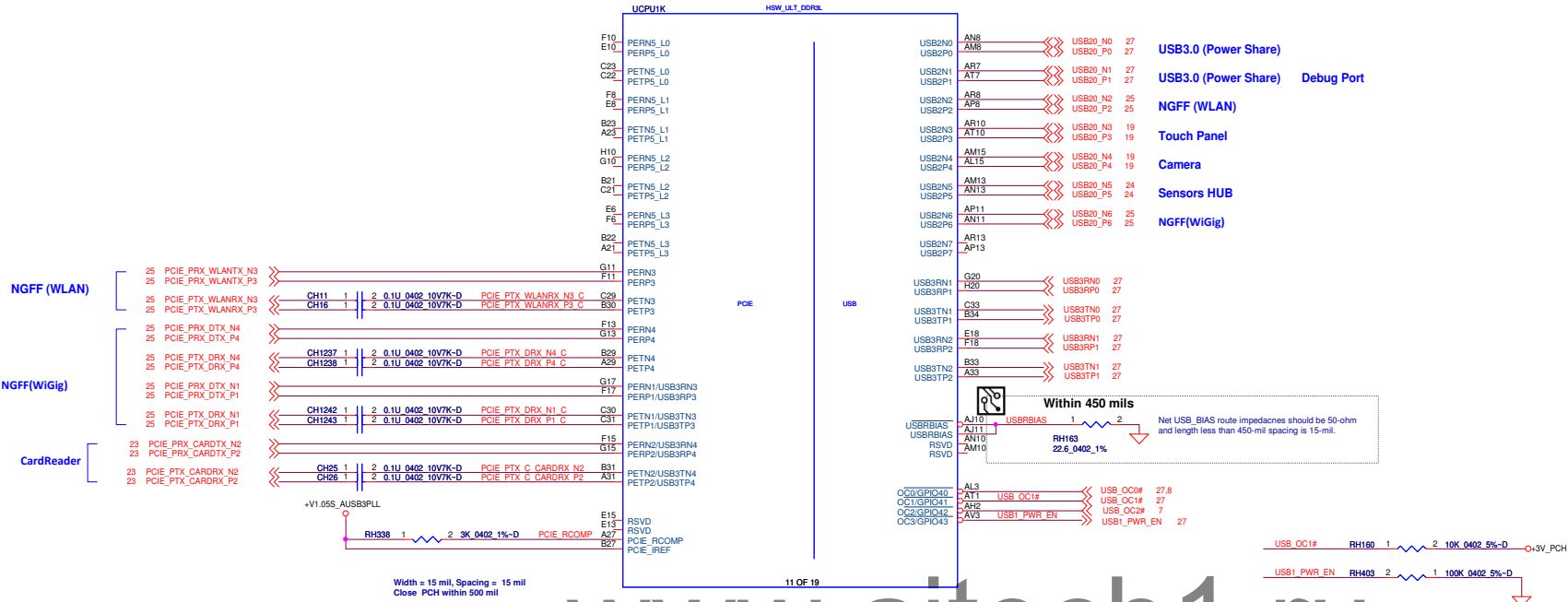


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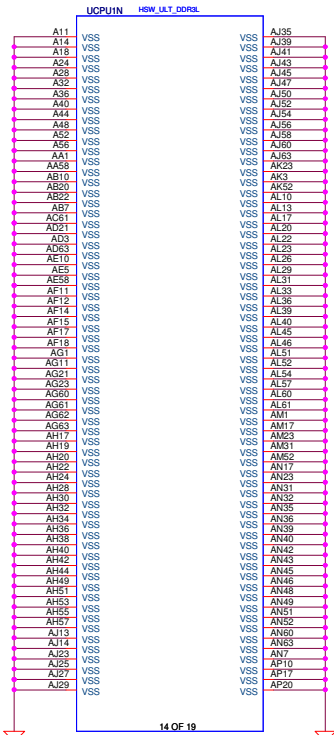
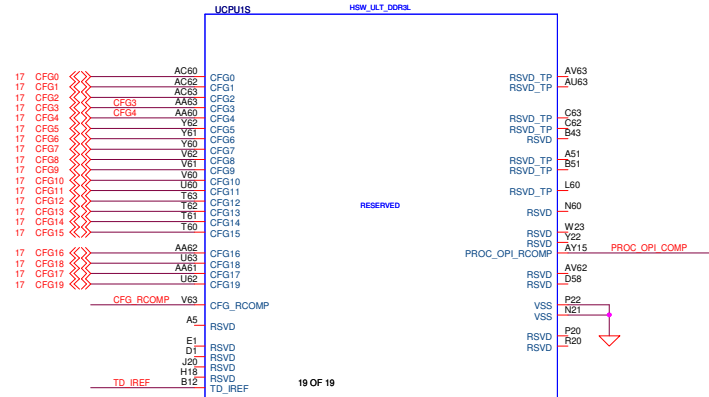
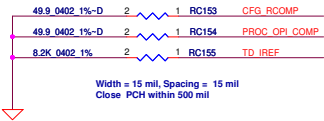
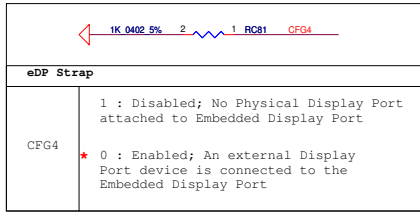
TPM BOM Optional

TPM	1 = W/TPM
	0 = W/O TPM

Security Classification	Compal Secret Data	Deciphered Date	2013/10/28	Title	P08-MCP(4/7) PM,GPIO,LPIO,MISC
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				LA-A161P	
				Date: Wednesday, August 14, 2013	
				Sheet 9 of 49	



follow INTEL PDG

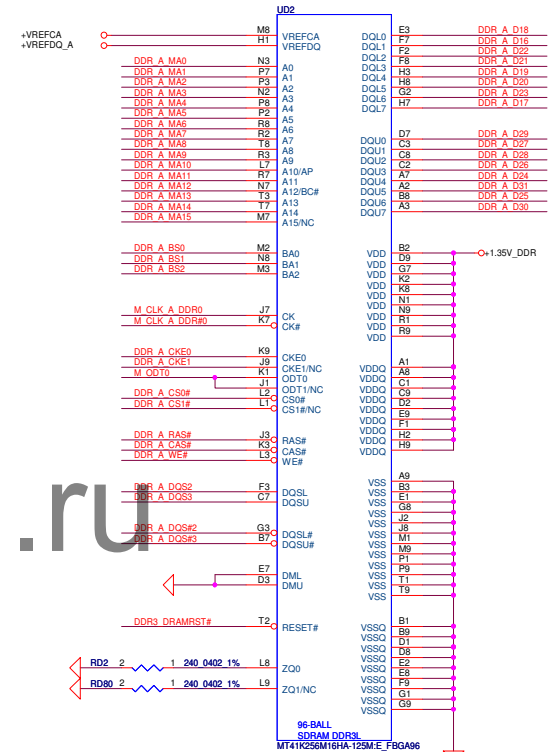
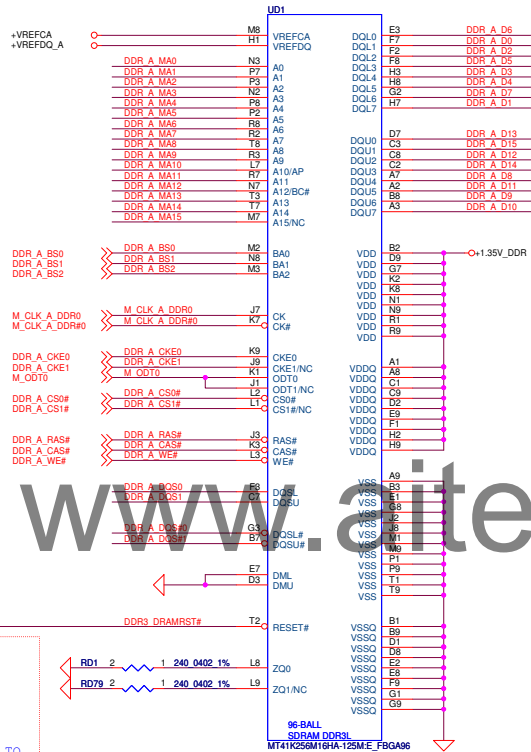


PLACE THESE CAPS
NEAR TO RESPECTIVE DRAM

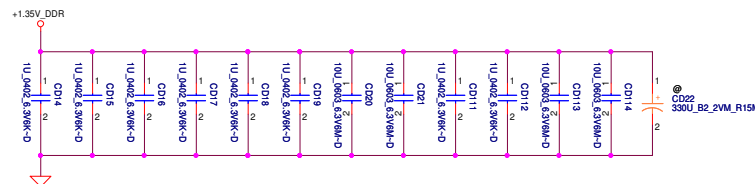


- 13.6 DDR_A_DQS#[0..7]
- 13.6 DDR_A_DQS[0..7]
- 13.6 DDR_A_D[0..63]
- 13.16.6 DDR_A_MA[0..15]

All VREF traces should
have 10 mil trace width



CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN



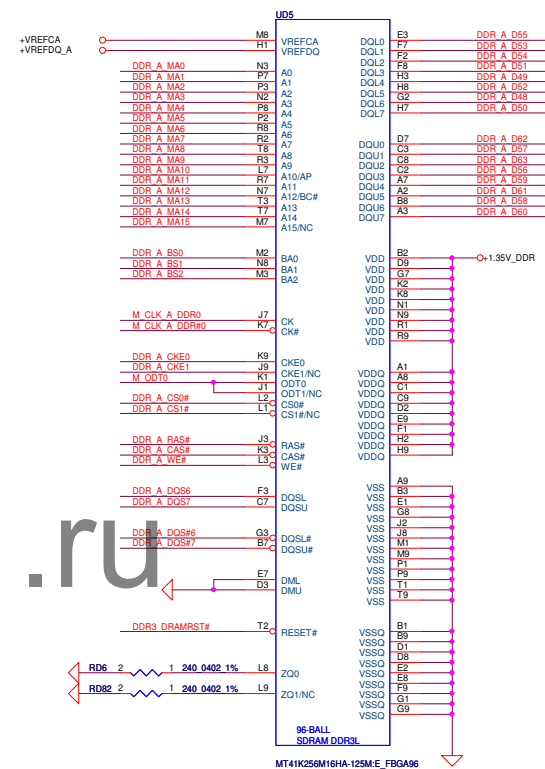
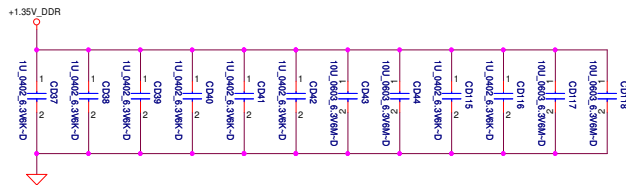
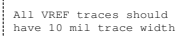
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title
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				LA-A161P
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				X02

follow INTEL PDG

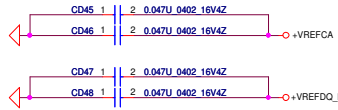
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CD25 2 0.047µs 0.0402 1.6V4Z
+VREFCA

CD26 1 2 0.047µs 0.0402 1.6V4Z
CD27 2 0.047µs 0.0402 1.6V4Z
+VREFDQ_A

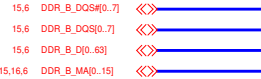
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NEAR TO RESPECTIVE DRAM**



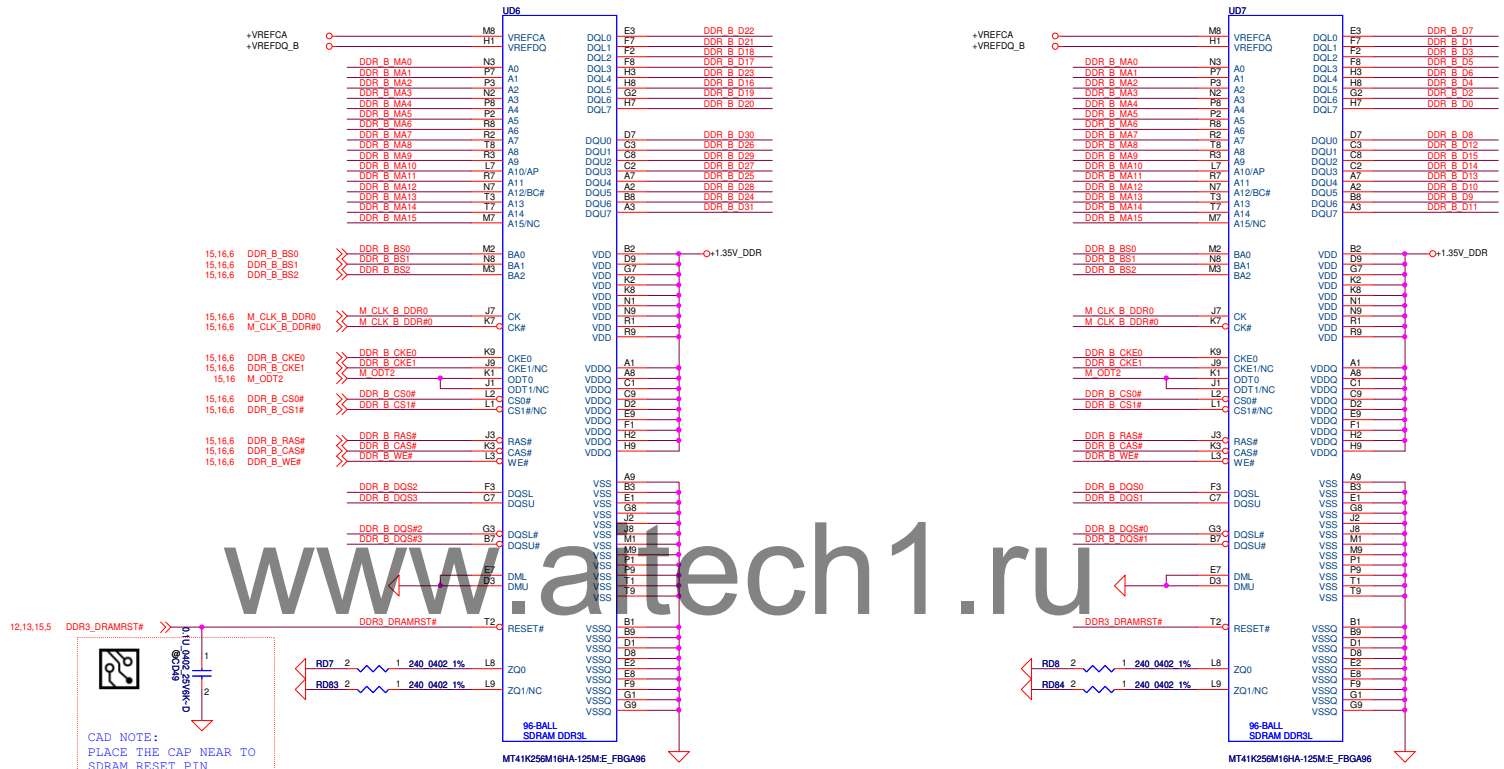
follow INTEL PDG



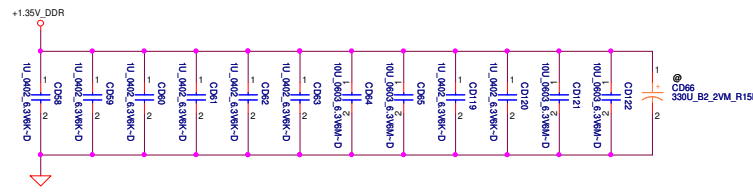
PLACE THESE CAPS
NEAR TO RESPECTIVE DRAM



All VREF traces should
have 10 mil trace width

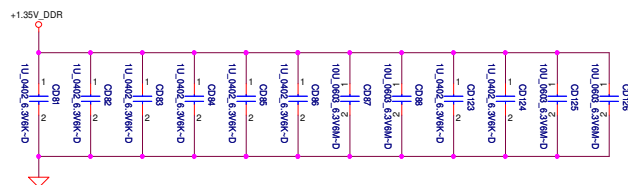
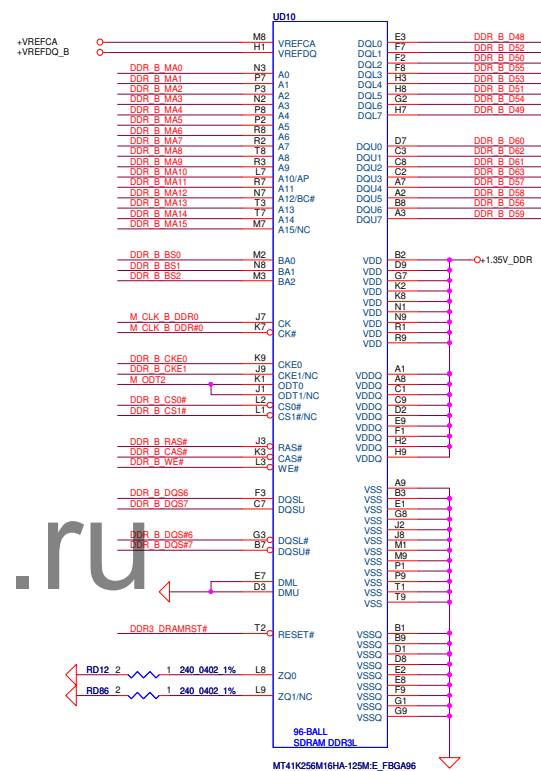
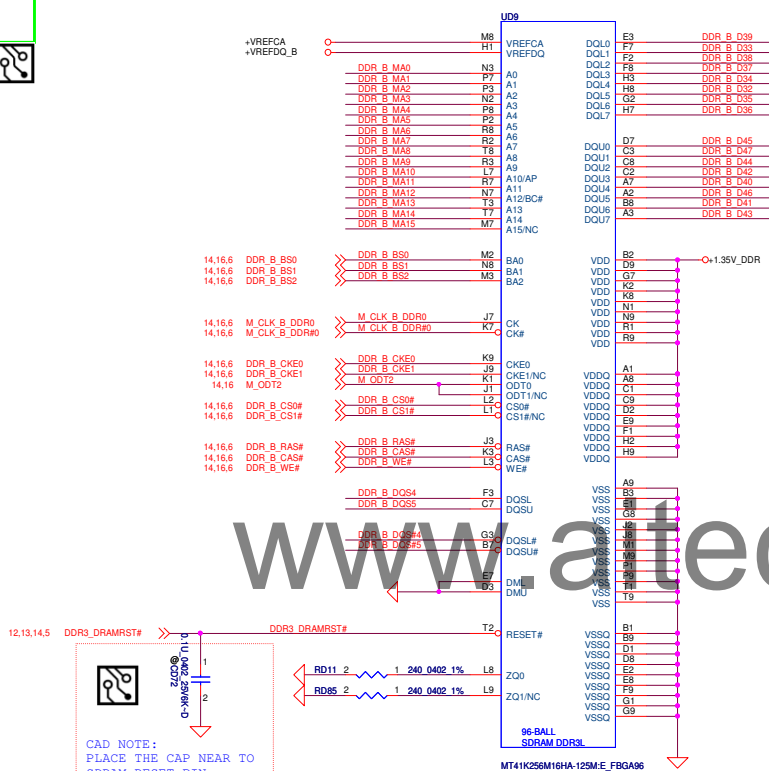


CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN



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		Size		LA-A161P	
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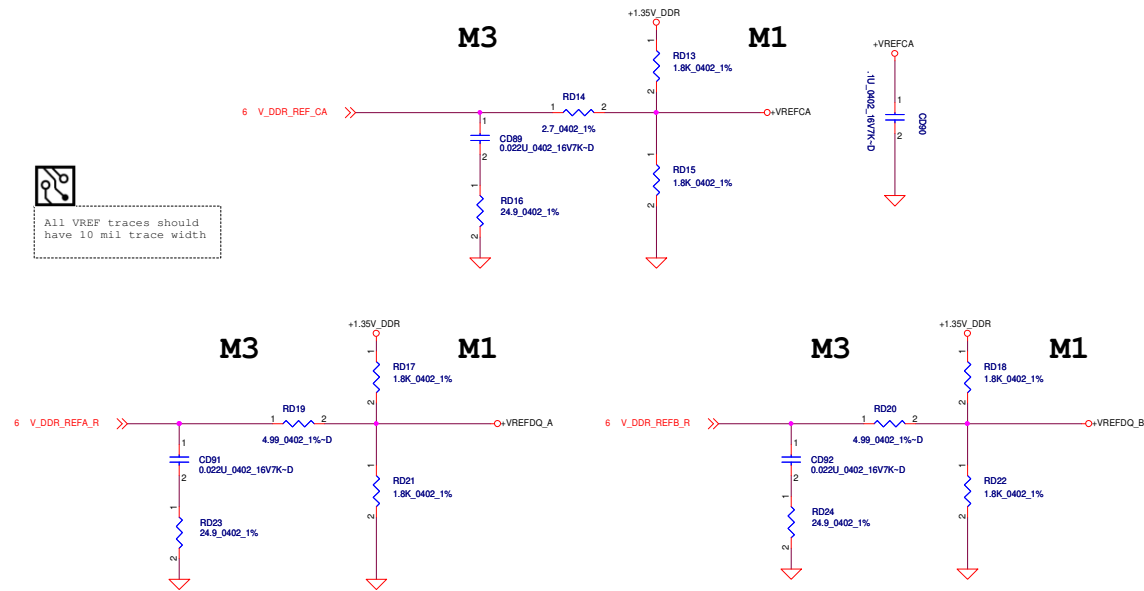
All VREF traces should have 10 mil trace width



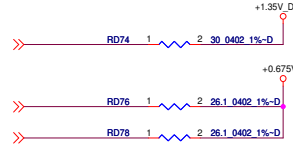
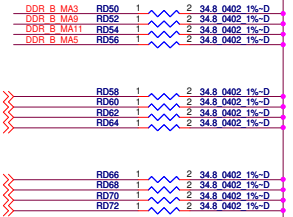
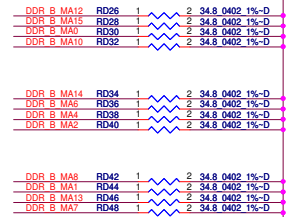
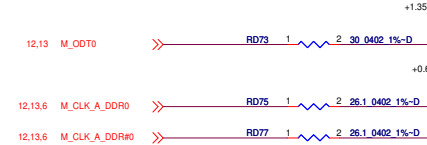
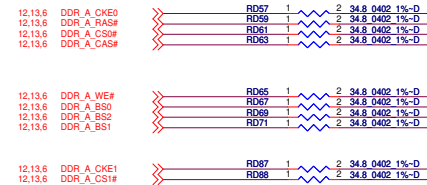
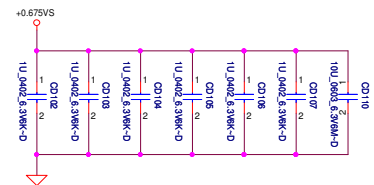
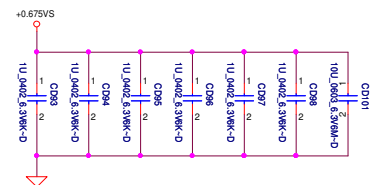
Security Classification	Compal Secret Data			Compal Electronics, Inc. P15-DDRIII Channel B Upper		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title		
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All VREF traces should have 10 mil trace width

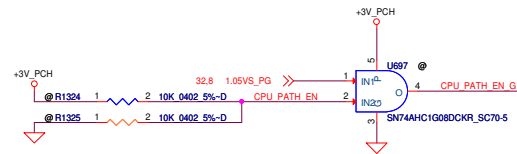


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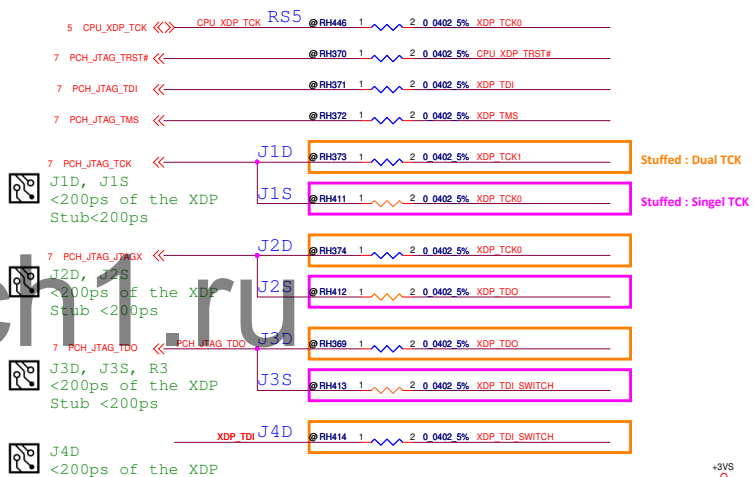
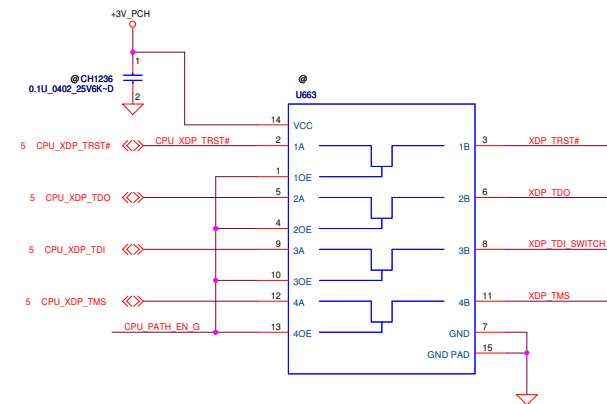


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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title
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Size				Document Number
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Date: Wednesday, August 14, 2013				A00
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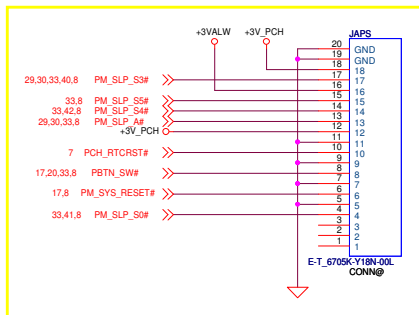
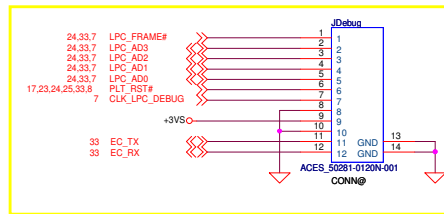
0806-16 NC the XDP control circuit for XB phase



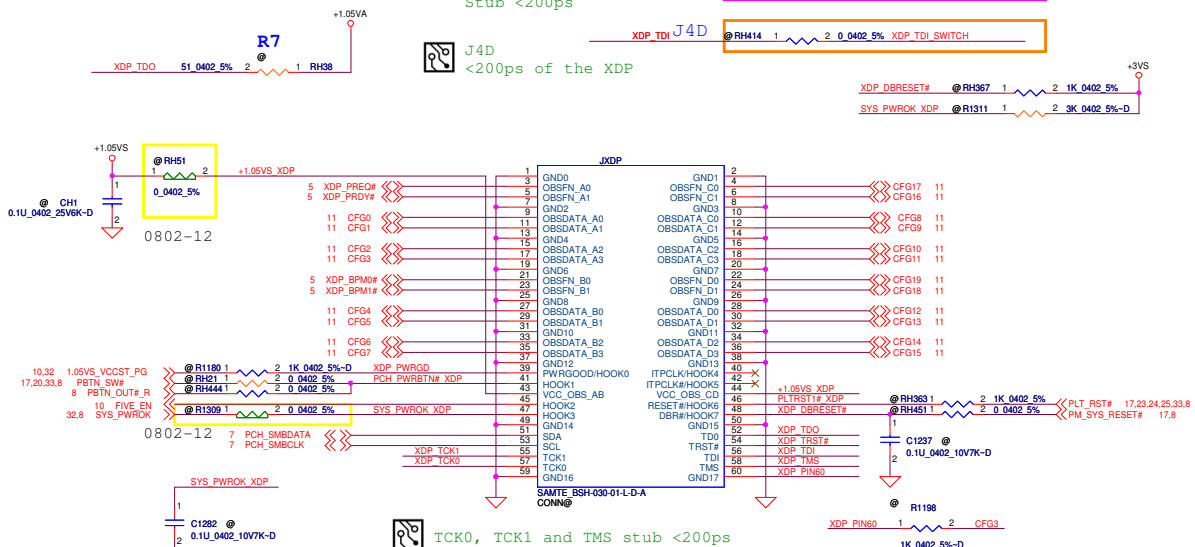
Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1, R2, J1d, J2d, J3d, J4d, R3, R4, R5	J1s, J2s, J3s
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan Manufacturing test	J1s, J2s, J3s, R3, R4, R5	R1, J1d, J2d, J3d, J4d



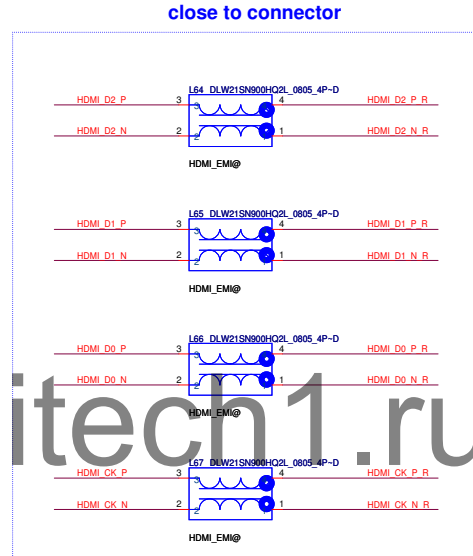
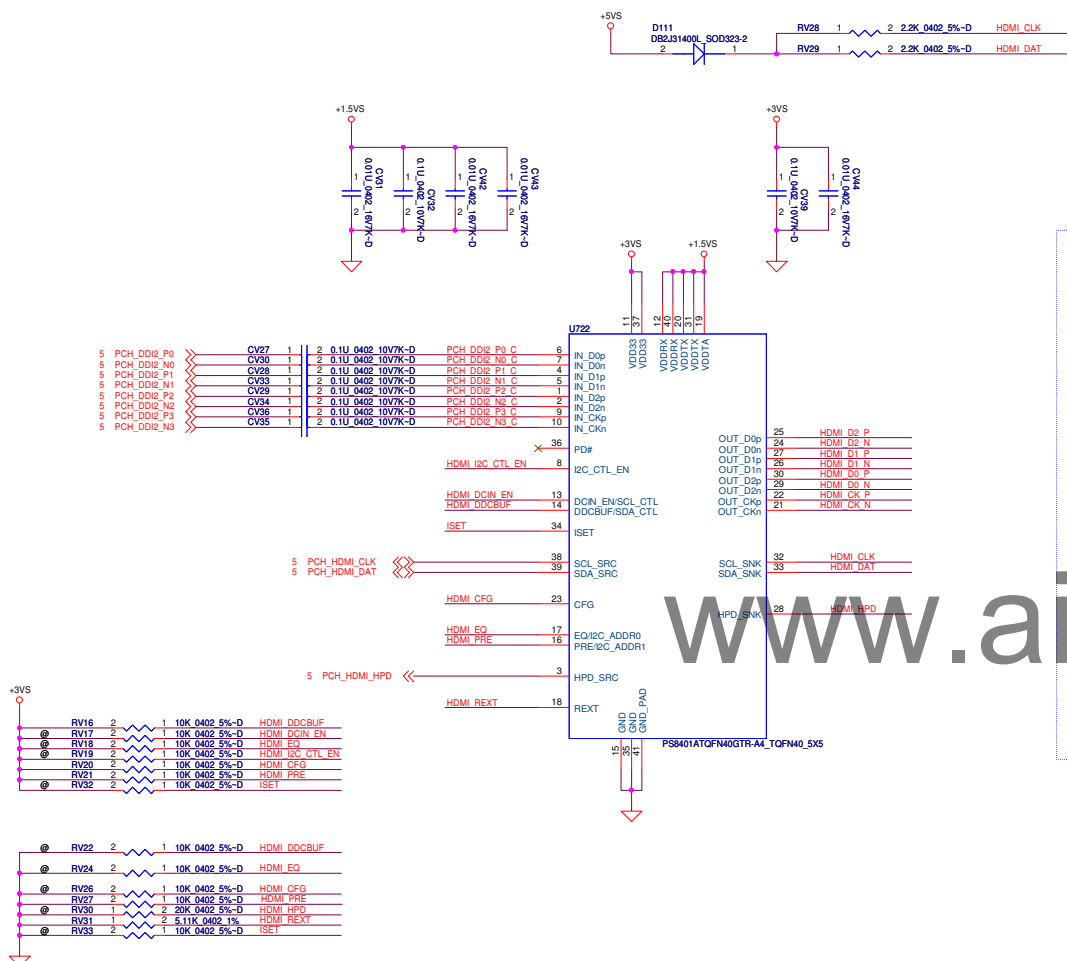
0806-18 NC the JDebug connector for XB phase



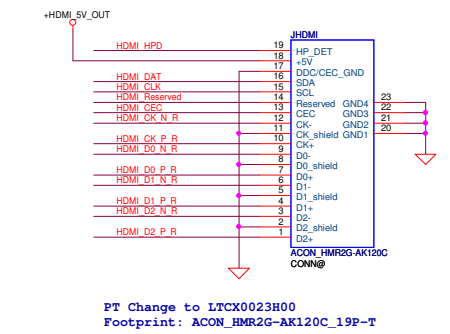
0806-18 NC the JAPS connector for XB phase



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		Date	Wednesday, August 14, 2013
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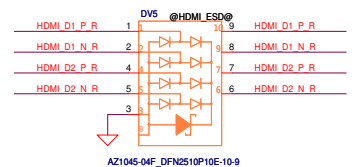
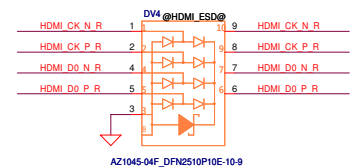
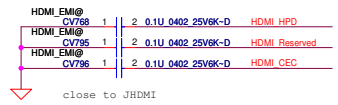


HDMI conn

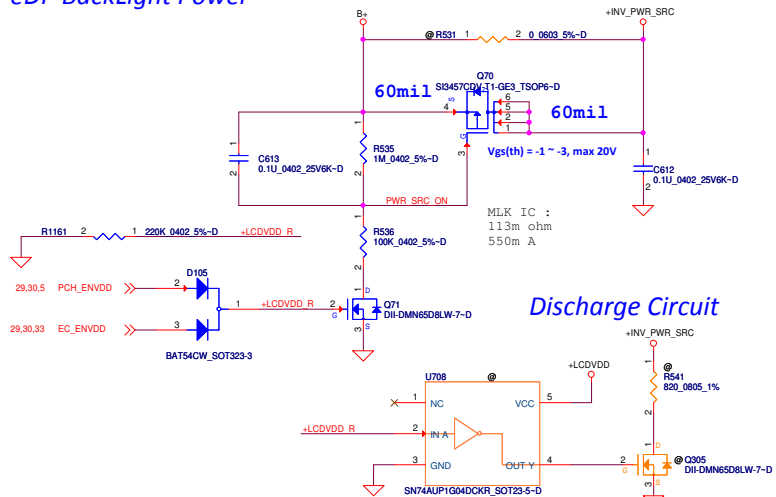


PT Change to LTCX0023H00
Footprint: ACON_HMR2G-AK120C_19P-T

For EMI Reserve

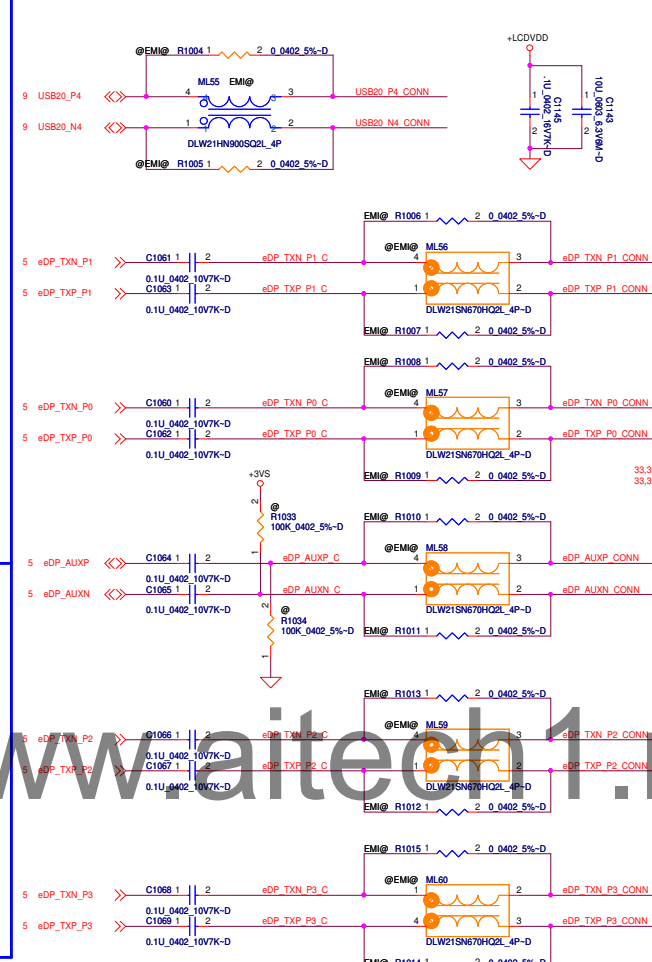
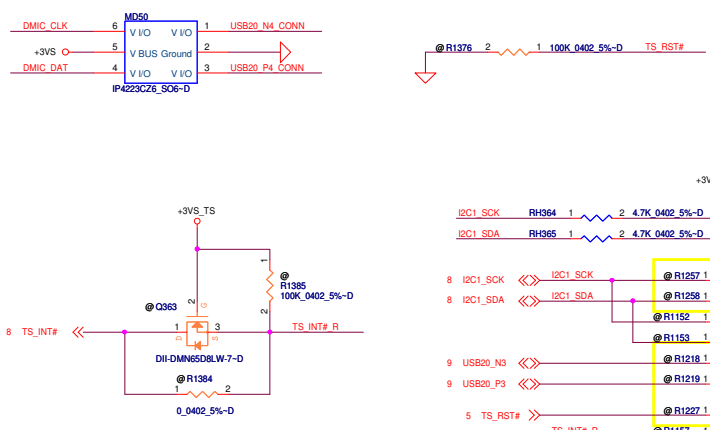
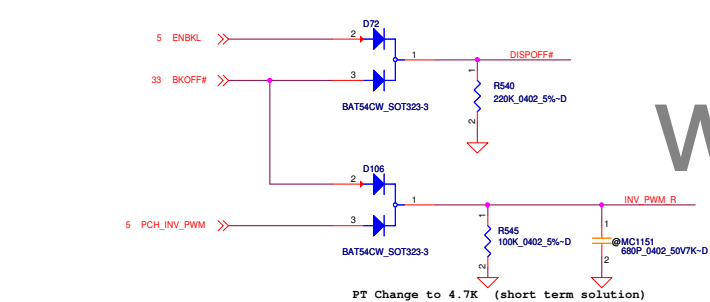


eDP BackLight Power

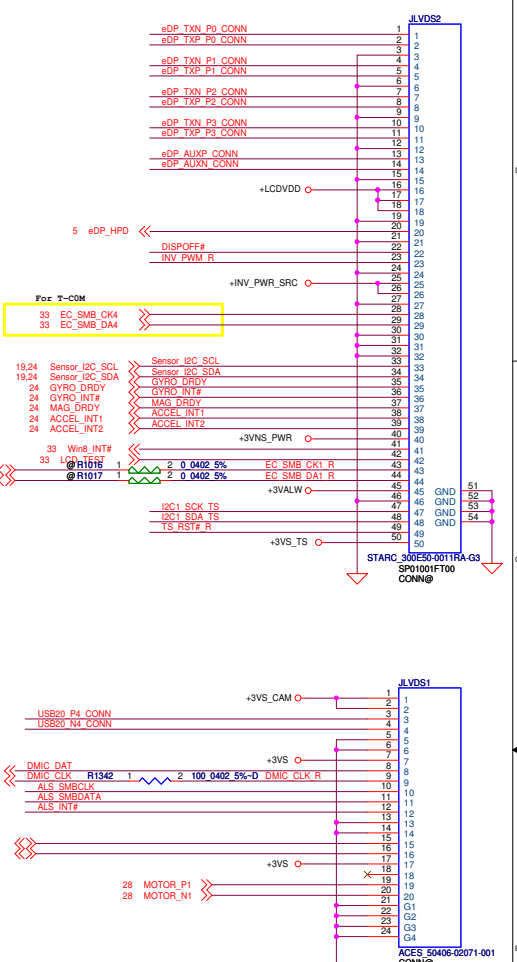


Discharge Circuit

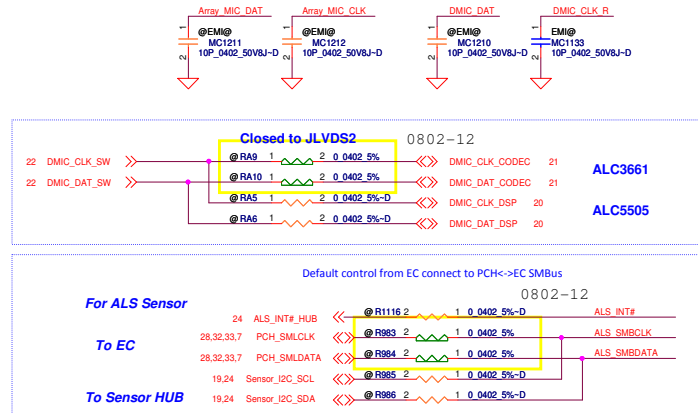
BackLight PWM Control



eDP Conn

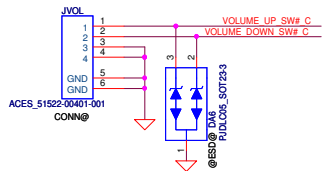


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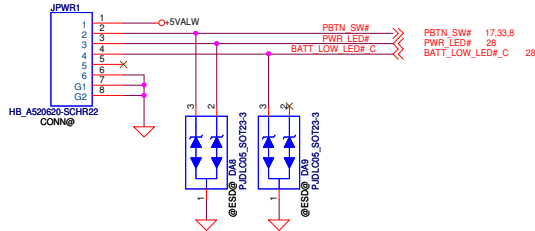


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		Size	19 of 49
		Date	Wednesday, August 14, 2013

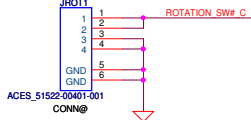
Volume Control Conn



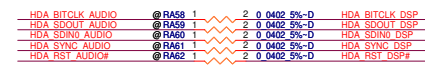
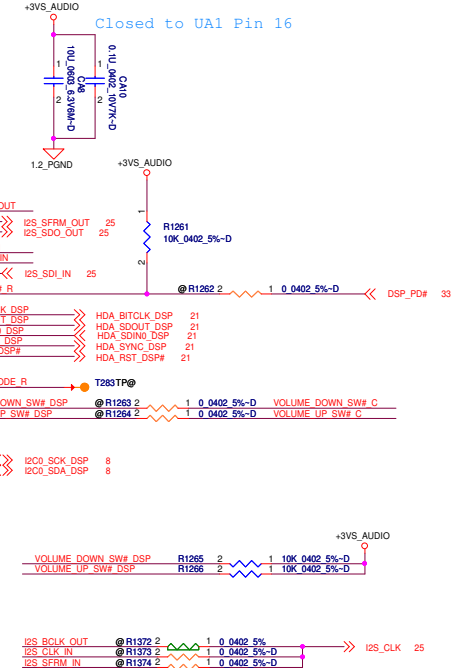
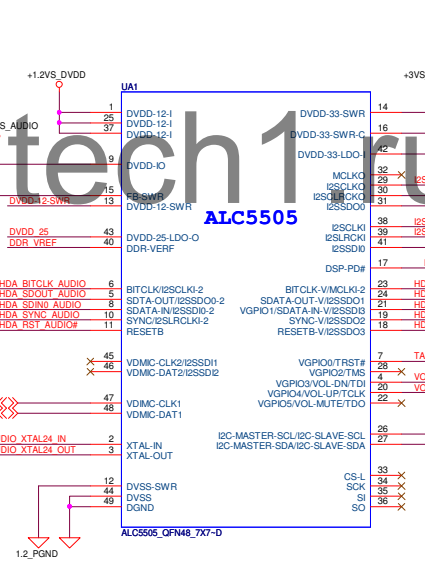
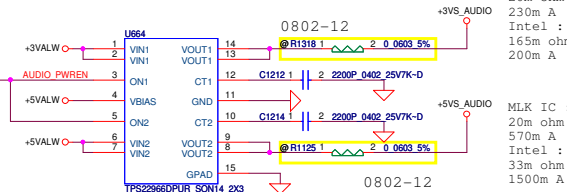
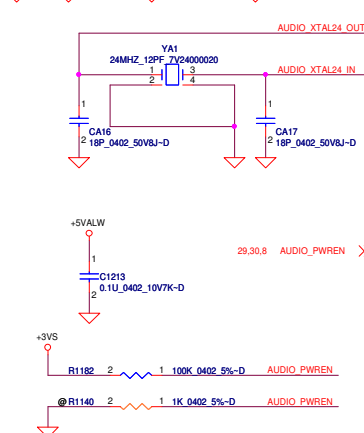
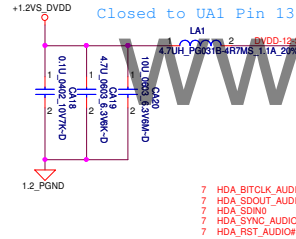
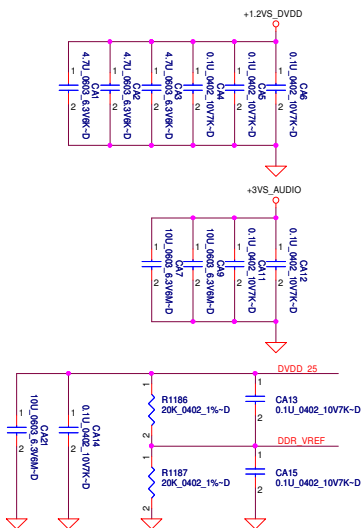
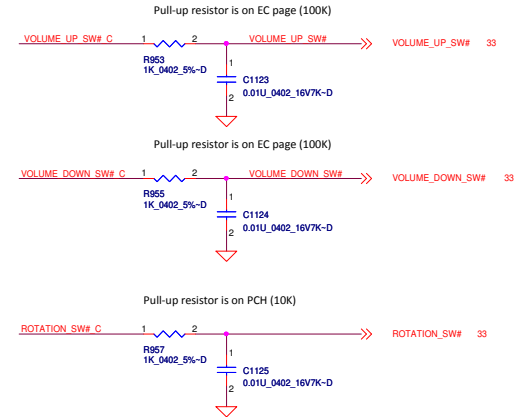
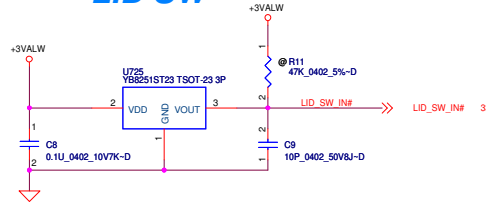
PWR Conn



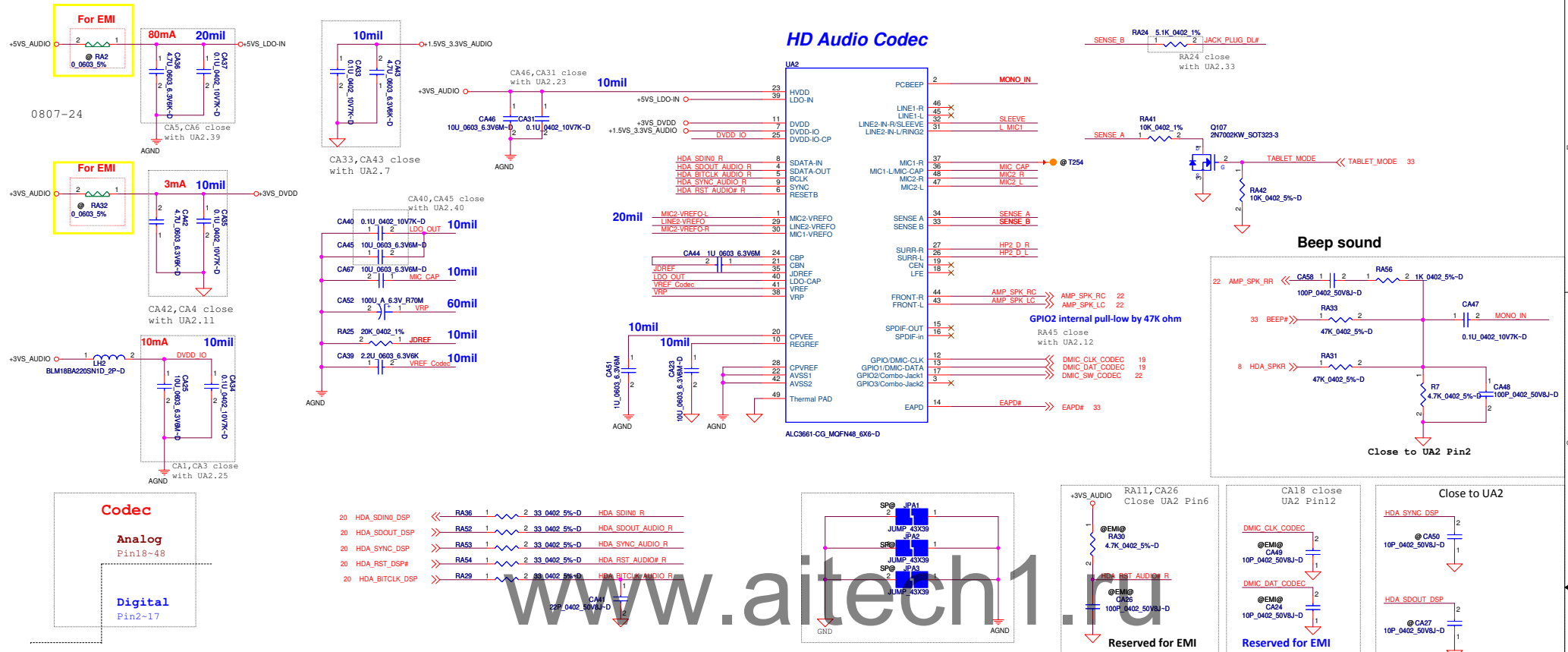
Hinge angle detect Conn

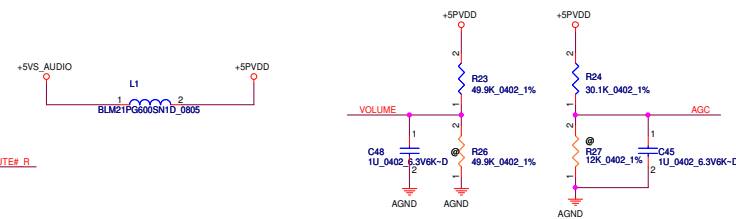
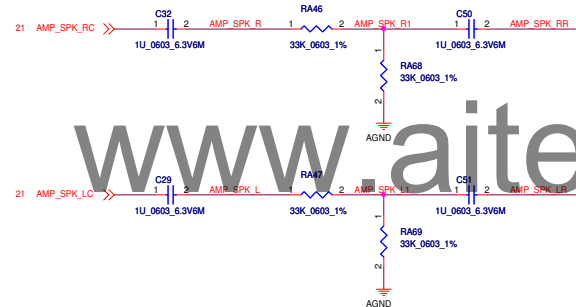
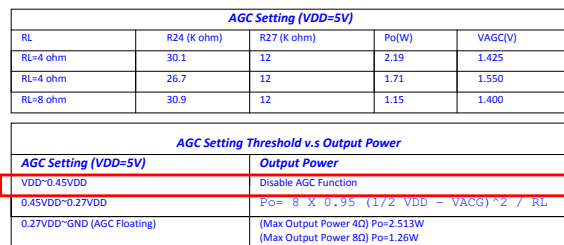
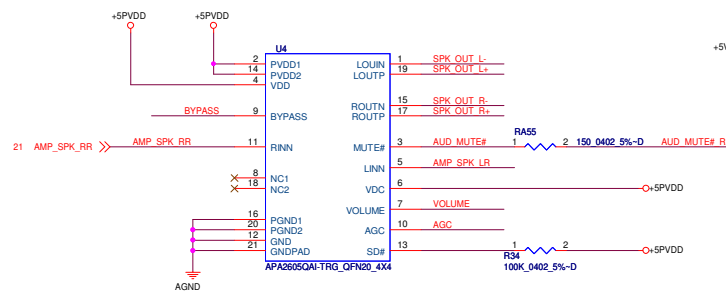


LID SW

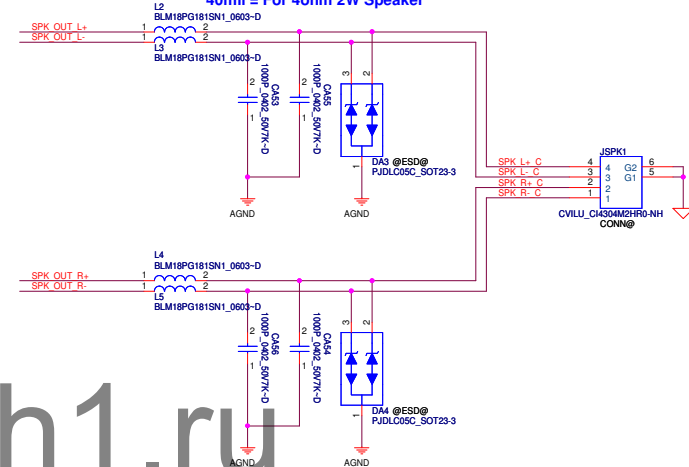


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40mil = For 4ohm 2W Speaker



C & 2nd D-MIC Switch

0812-27 Change to short pad

Security Classification	
Issued Date	20

THIS SHEET OF ENGINEERING DRAWING IS

	DMIC-SW-DIS HI	DMIC-SW-DIS LOW
DMIC_SW_CODE is Hi	Q134, Q136 ON Q135 OFF BE2#/BE3# High BE0#/BE1# Low 2nd D-MIC	Q136, Q135 OFF Dis_connect
DMIC_SW_CODE is Low	Q135 ON Q134, Q136 OFF BE2#/BE3# Low BE0#/BE1# High Web D-MIC	Q136, Q135 OFF Dis_connect

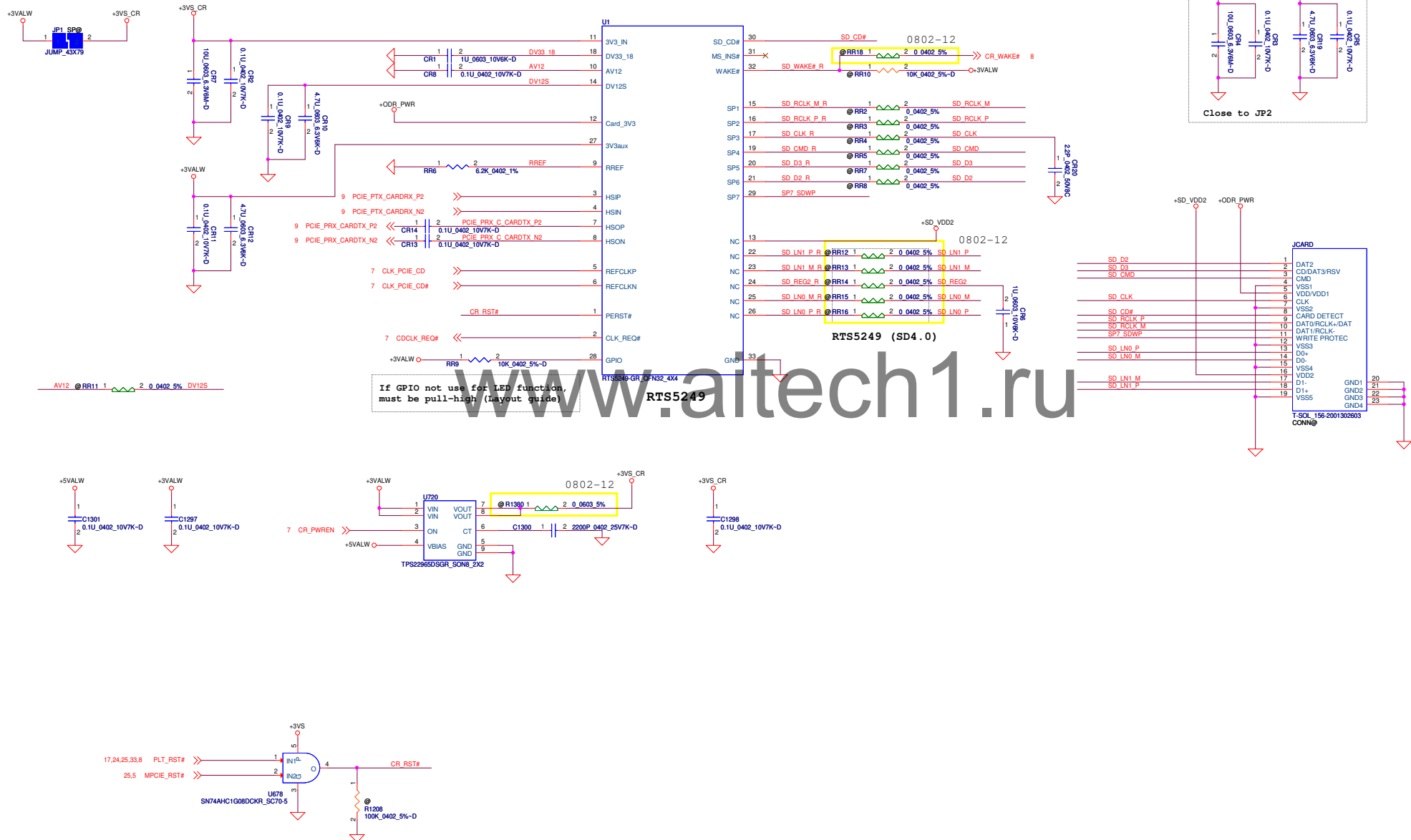
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title P22-Audio DSP, IOL Conn		
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Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.

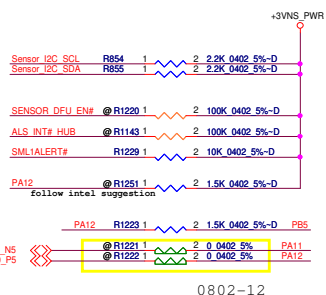
```
Support Runtime D3 mode
=> unstuff:JP1,RR10
```

```
Not Support Runtime D3 mode
=> unstuff:U720,R1380,C1300
    stuff:JP1,PP10.
```



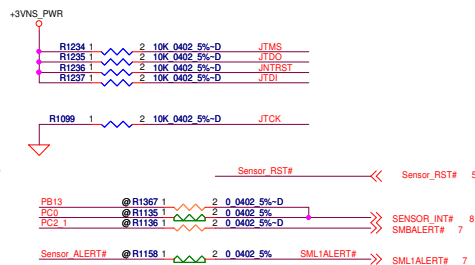
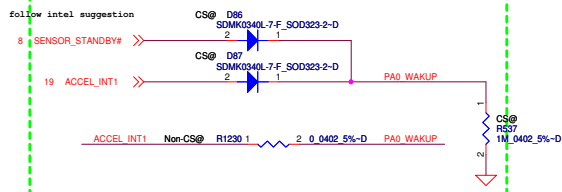
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					LA-A161P	A00	
				Date:	Wednesday, August 14, 2013	Sheet	23 of 49

Sensor Fussion

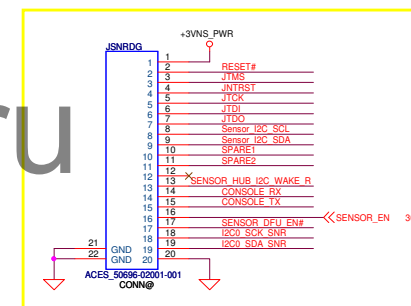
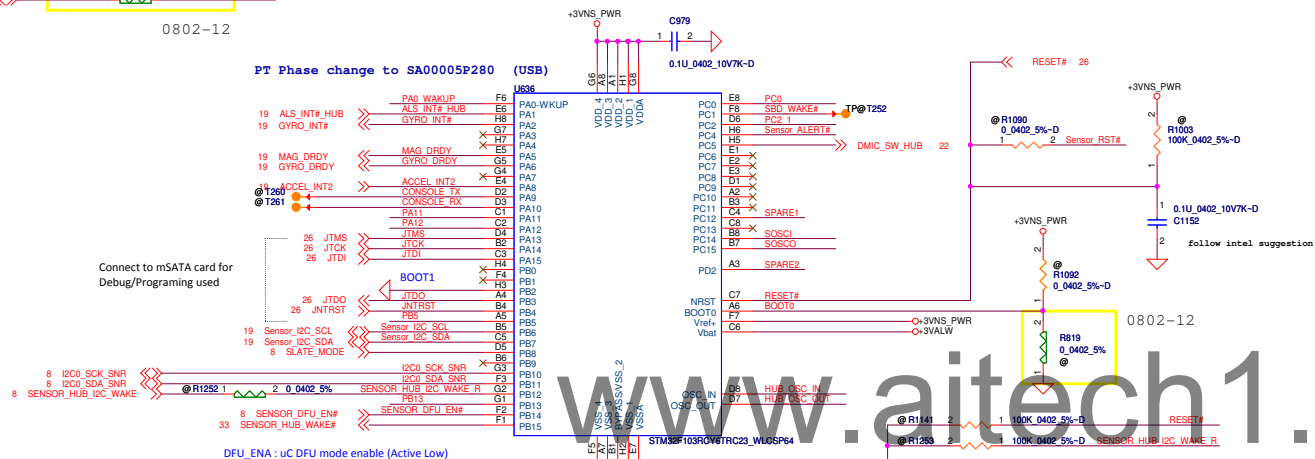


0802-12

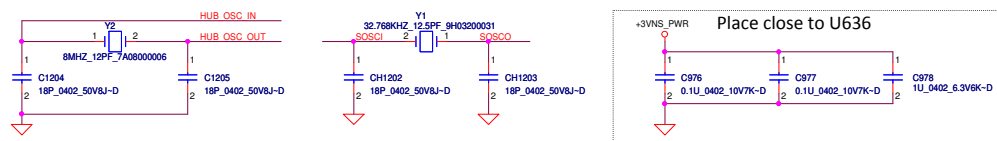
CS & Non-CS option



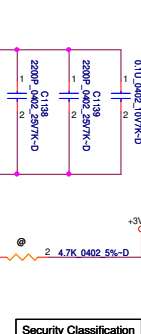
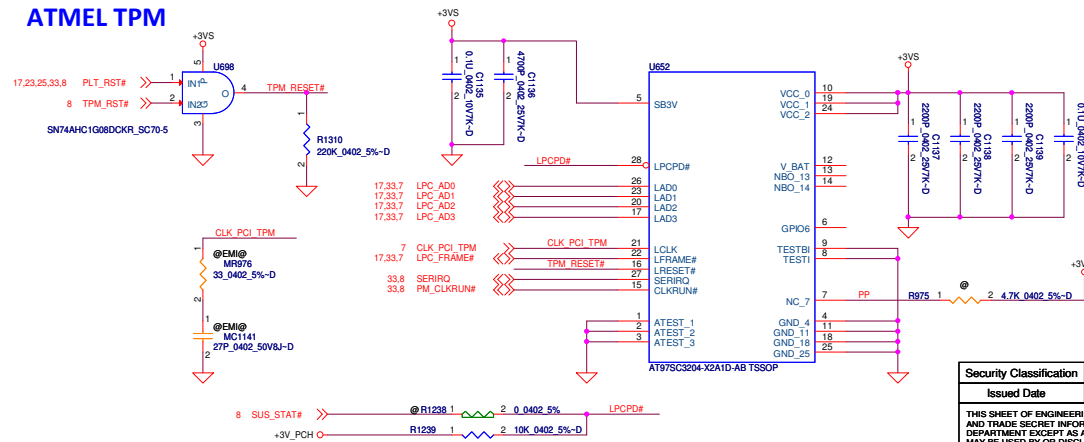
Note :
Sensor Part Number
CS@: SA00005P23L
Non-CS@: SA00005P250 P/N:STM32F103RCY6TRC28



0806-19 NC the JSNRDG connector for XB phase

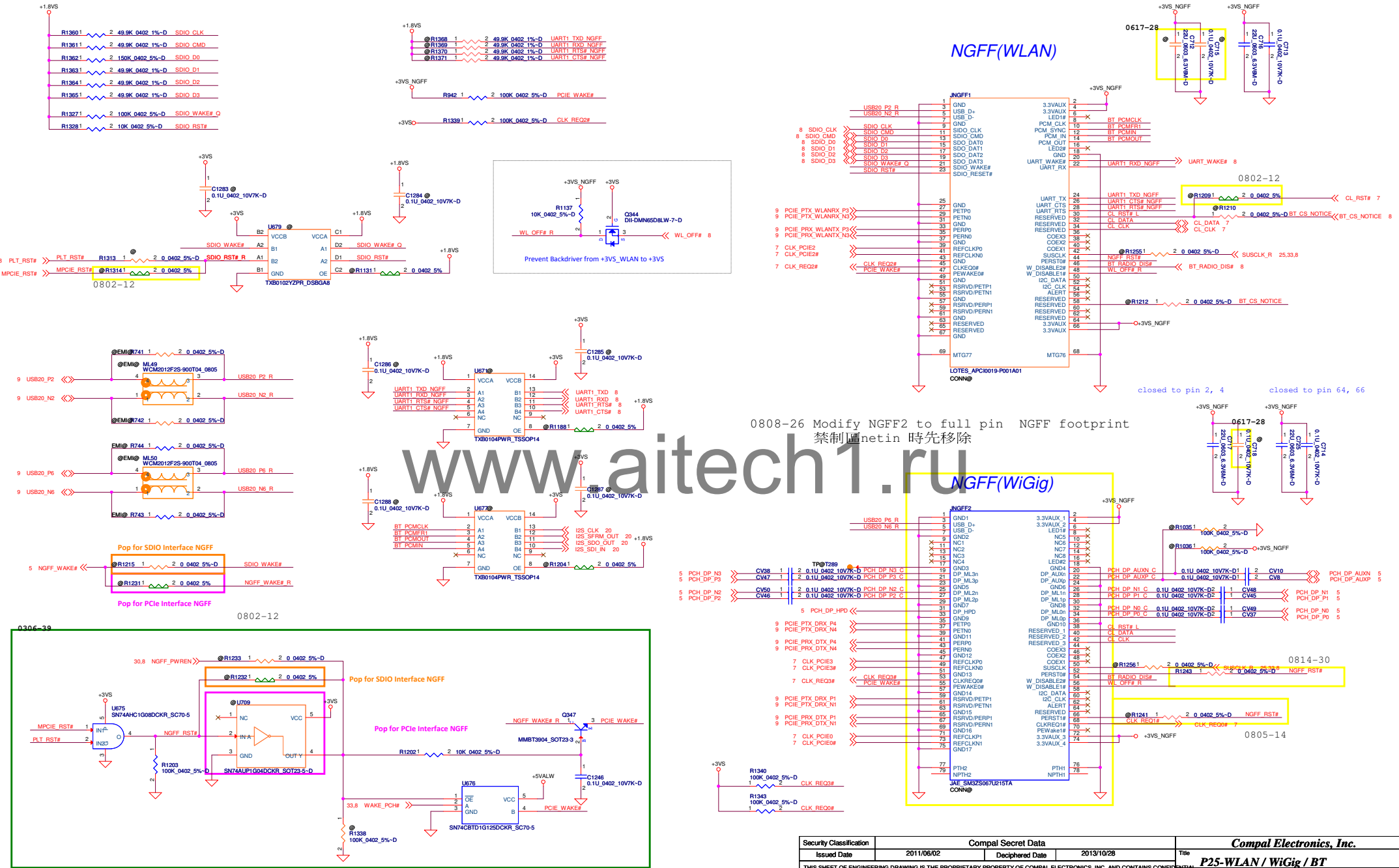


ATMEL TPM



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				Size	Document Number	Rev A
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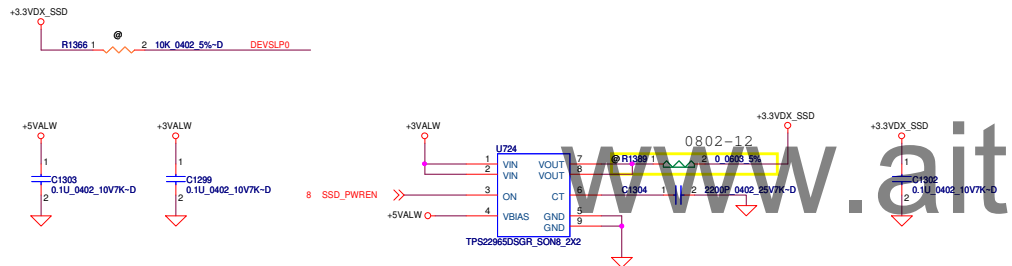
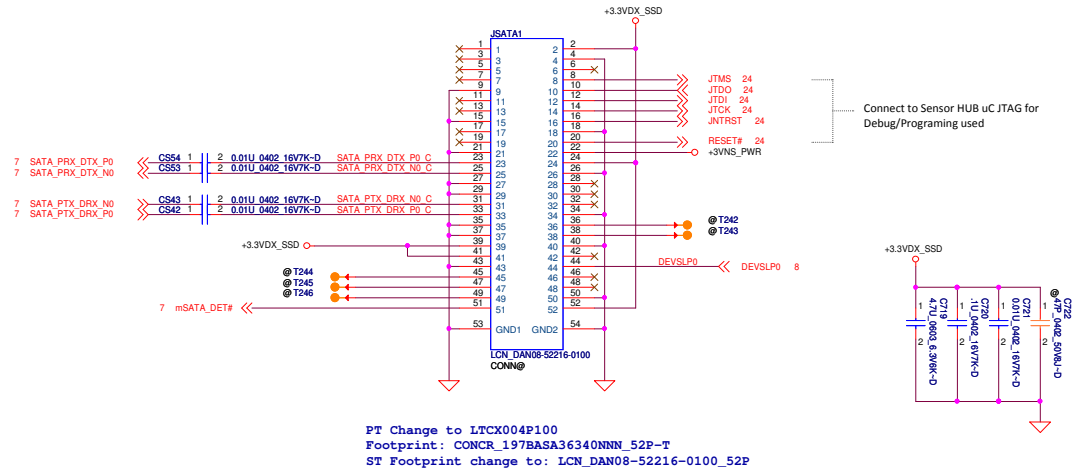
Wireless LAN



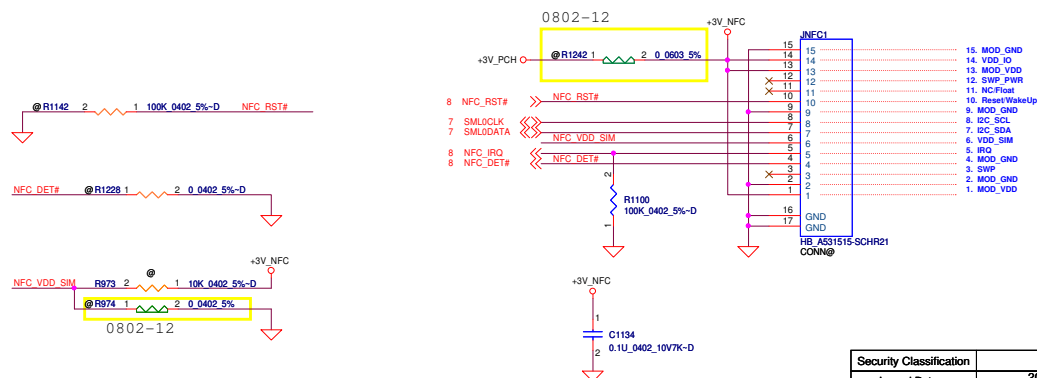
0808-26 Modify NGFF2 to full pin NGFF footprint
禁制圖netin 時先移除

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mSATA Card

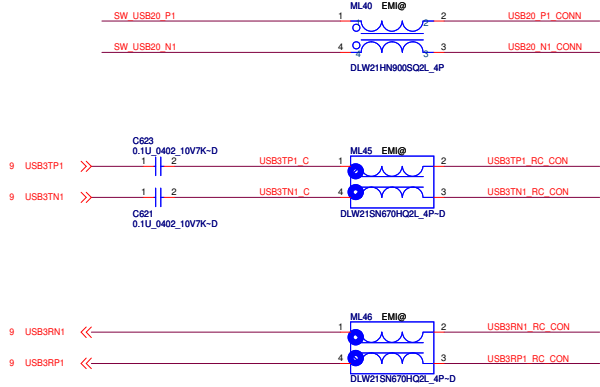


ME Decide using 15 pin conn
MB 15 <-----> 15 pin NFC
The I2C address set on the module is 28h



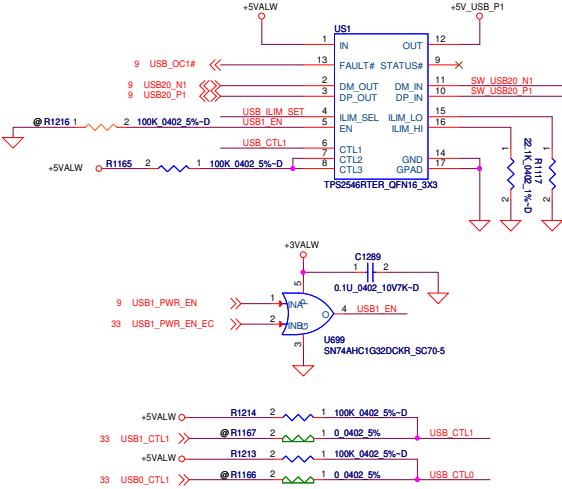
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2011/06/02		2013/10/28		P26-mSATA / NFC Conn	
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C		Document Number		LA-A161P	
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USB IO Port

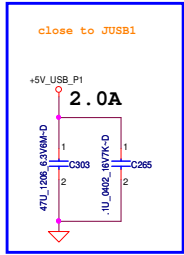
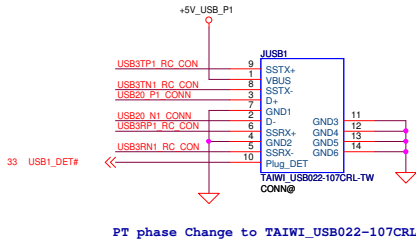


CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

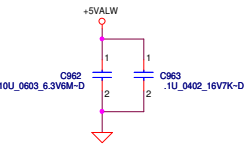
2.1A / Channel



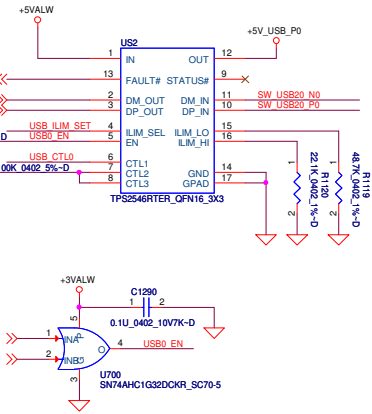
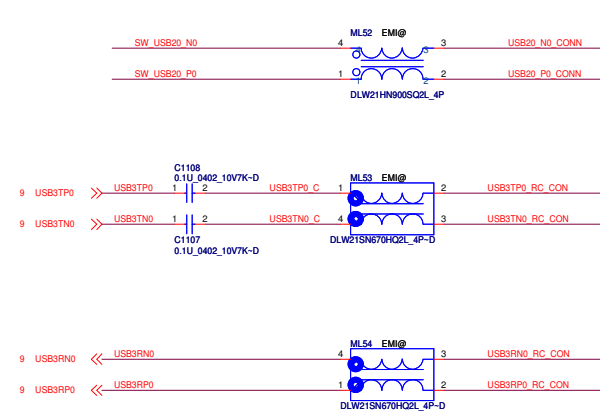
USB CONN



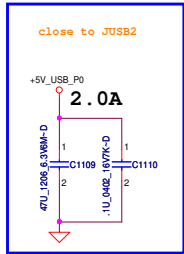
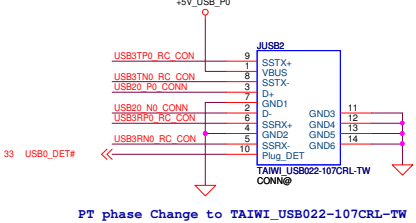
For ESD request



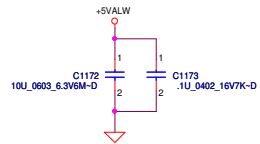
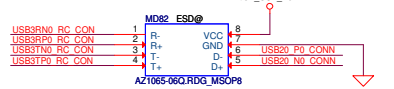
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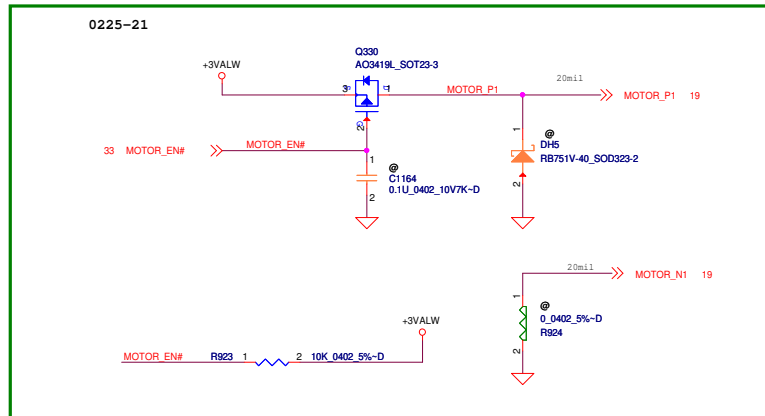
USB CONN



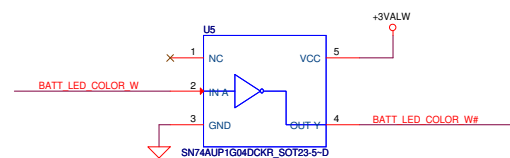
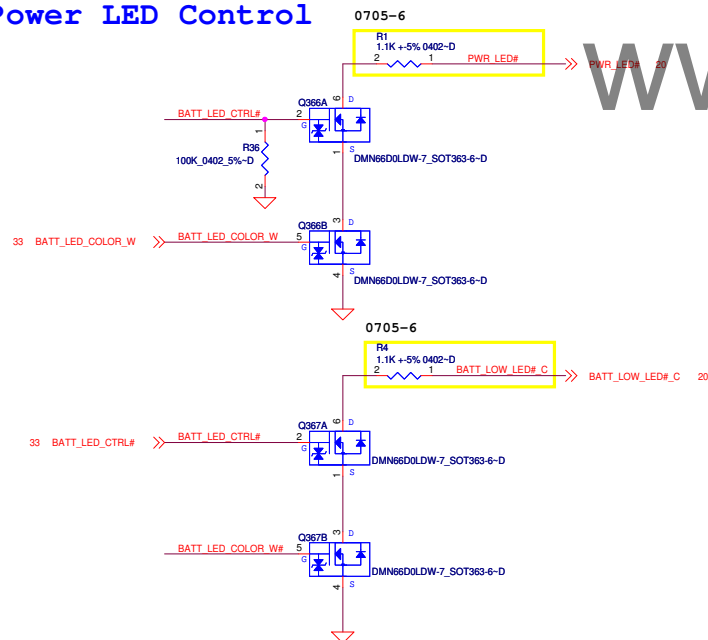
For ESD request



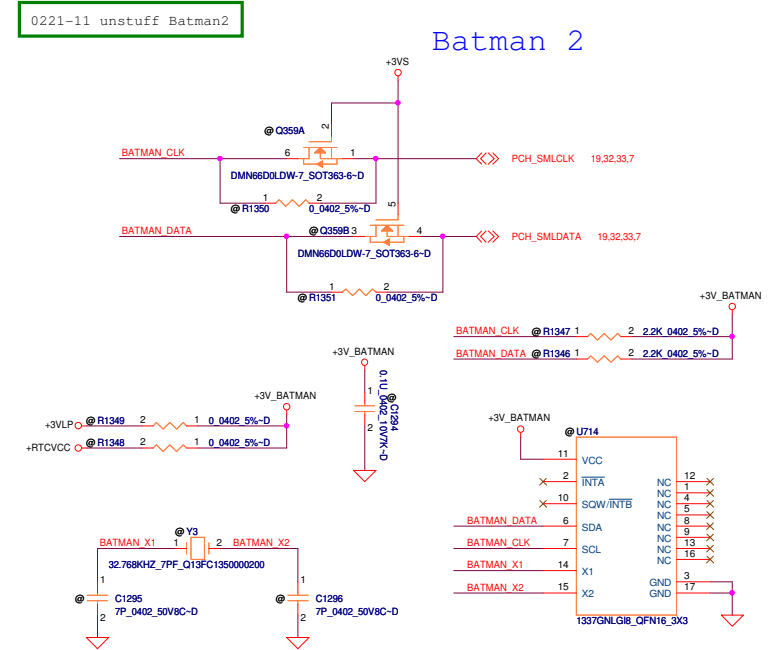
Vibrator



Power LED Control

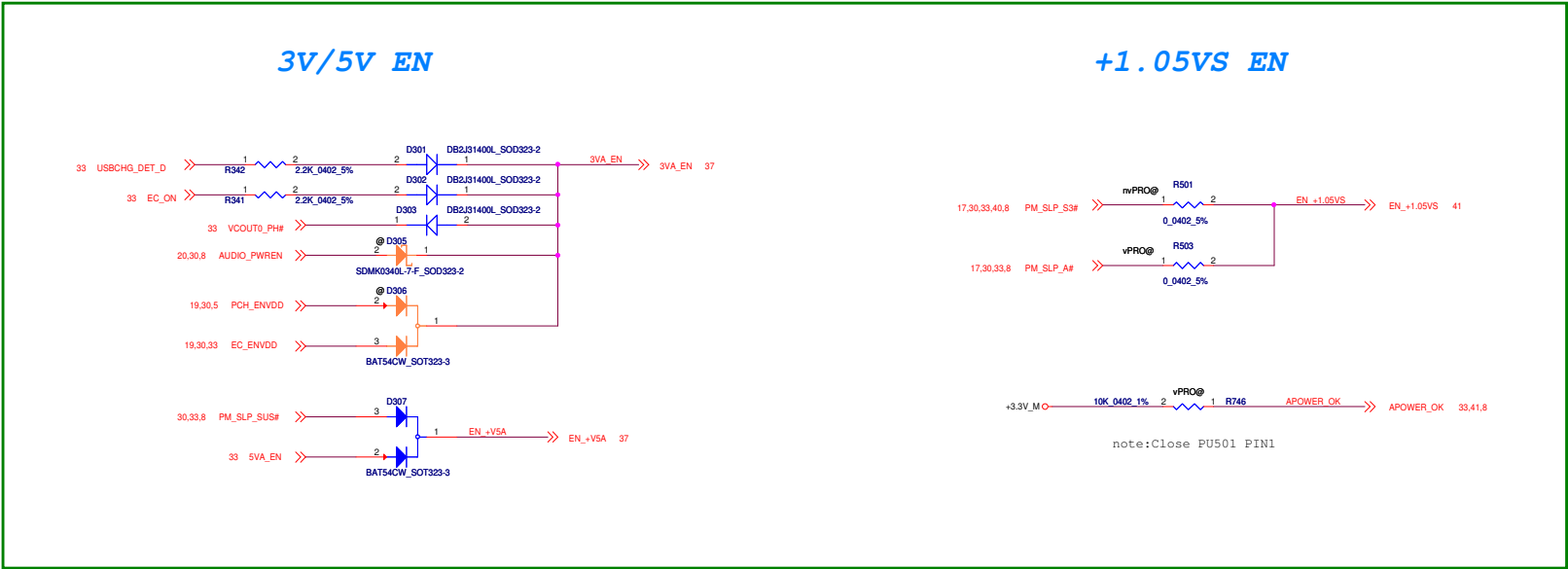


Batman 2

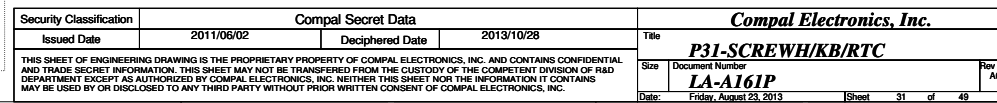


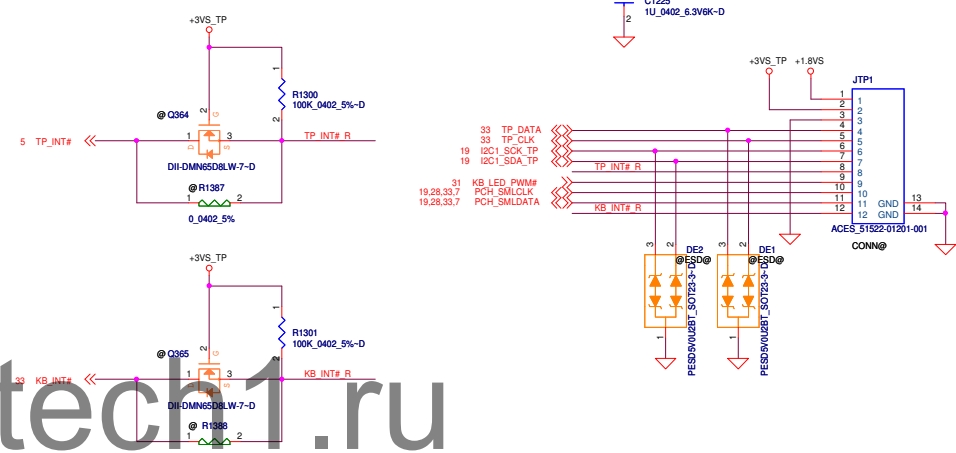
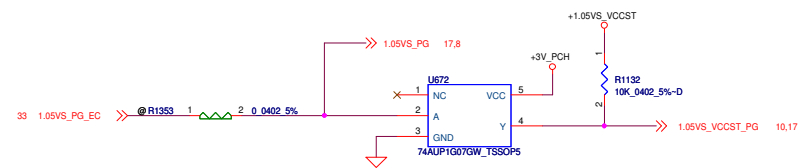
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Issued Date		2011/06/02	Deciphered Date	2013/10/28	Title		
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					Size	Document Number	Rev
					Date:	Wednesday, August 14, 2013	Sheet
					LA-A161P		
					A00		

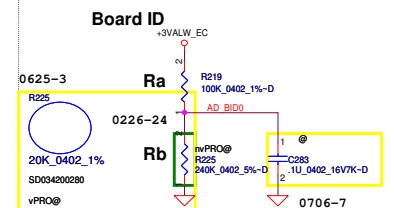
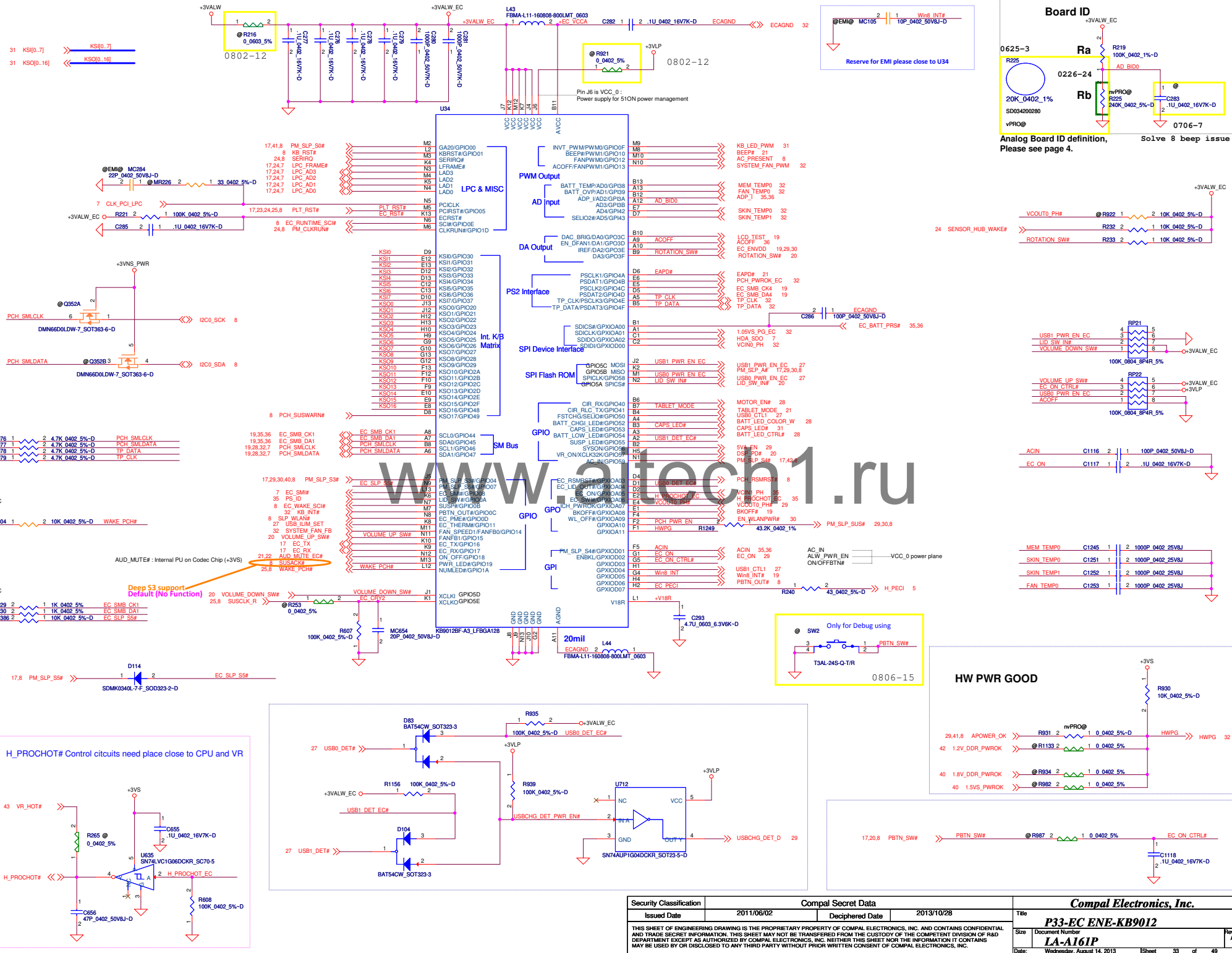


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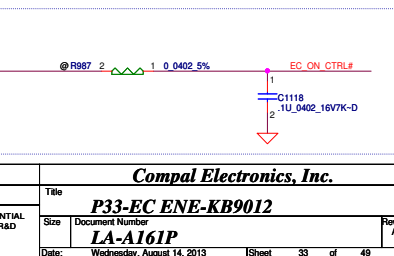
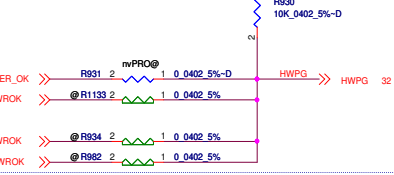
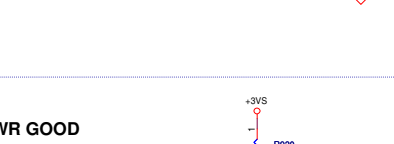
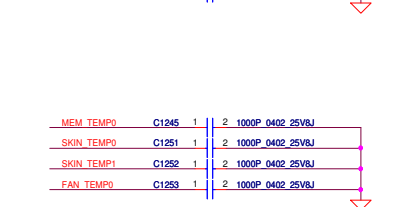
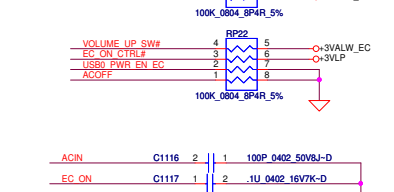
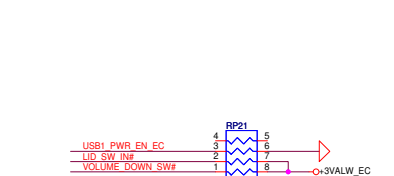
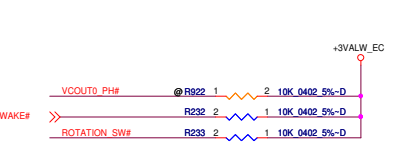




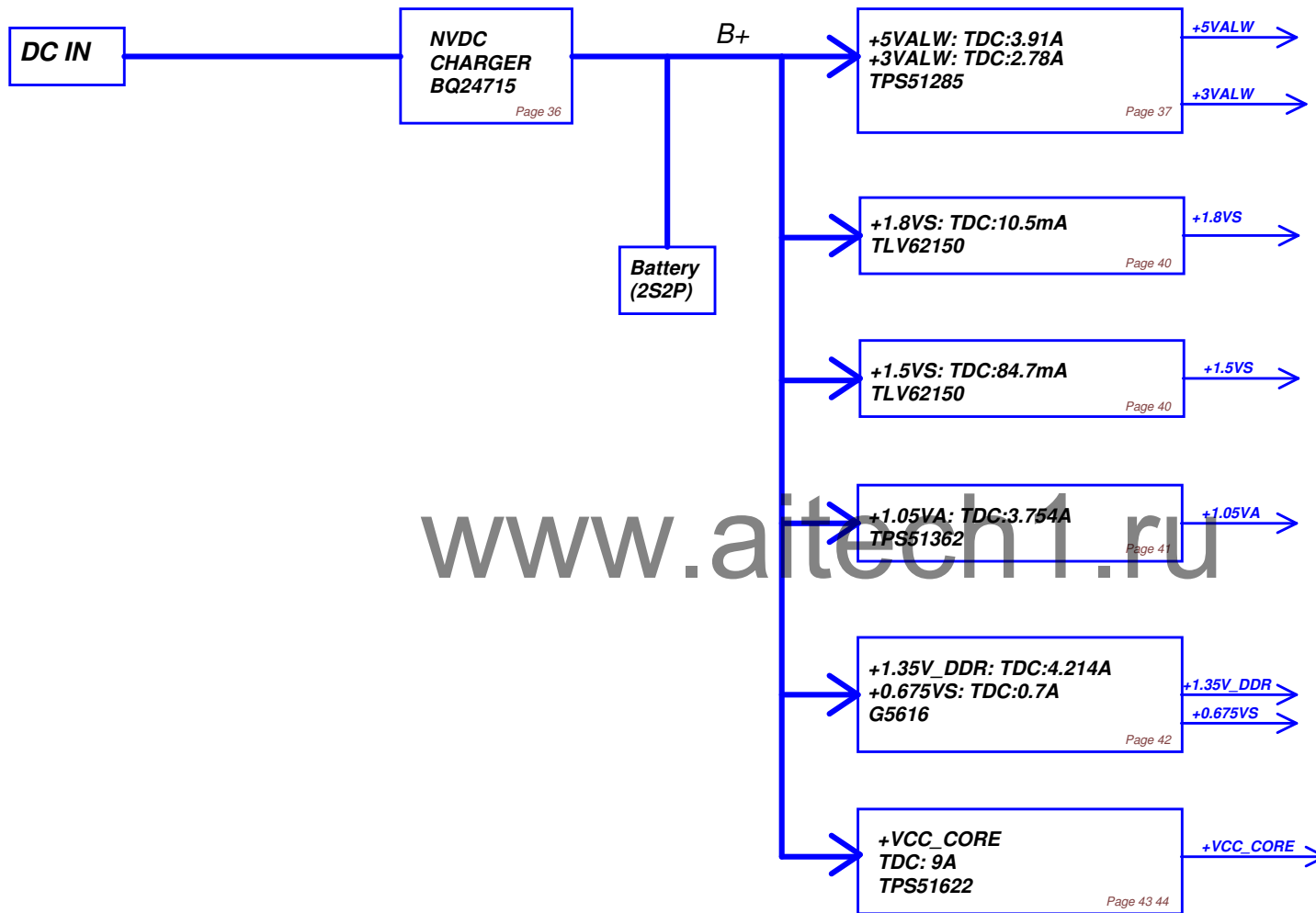
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P32-TP / FAN/PWGERGD
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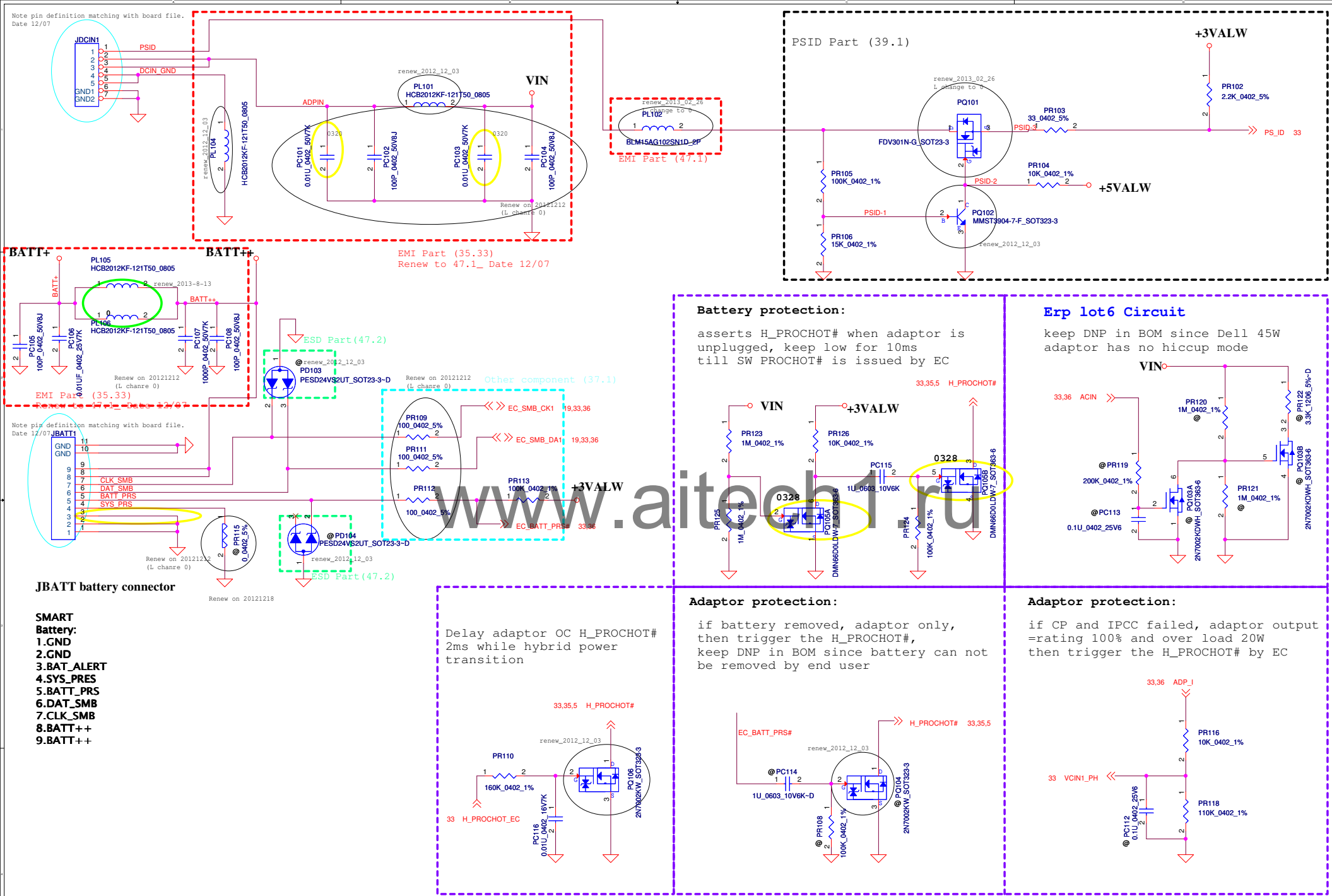
Analog Board ID definition, Please see page 4.



Security Classification	Compal Secret Data	Document Number	P33-EC ENE-KB9012
Issued Date	2011/06/02	Deciphered Date	2013/10/28
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		Date	Wednesday, August 14, 2013
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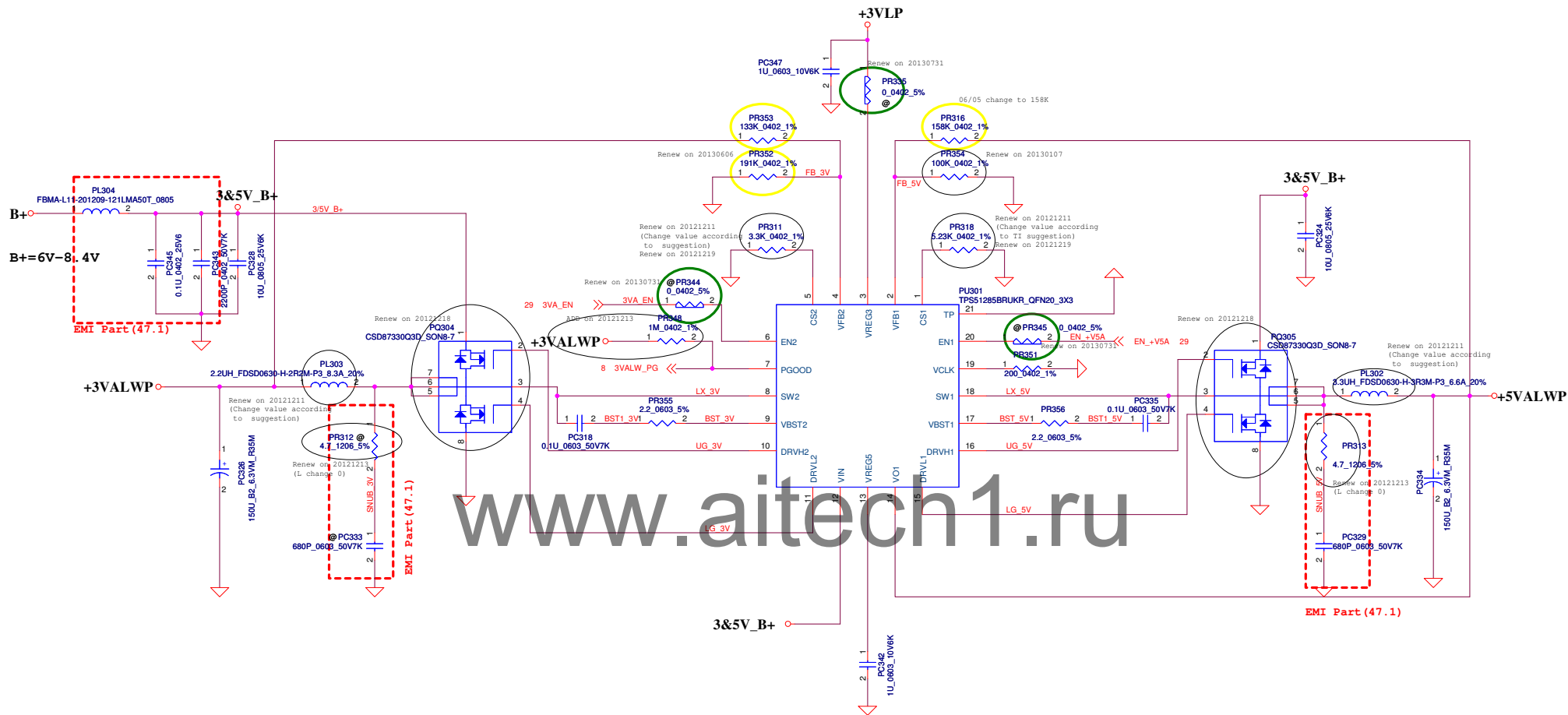
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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JBATT battery connector

- SMART
Battery:
- 1.GND
 - 2.GND
 - 3.BAT_ALERT
 - 4.SYS_PRES
 - 5.BATT_PRS
 - 6.DAT_SMB
 - 7.CLK_SMB
 - 8.BATT++
 - 9.BATT++

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P35-PWR DCIN/BATT CONN/OTP
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+3VALWP 1 @P304 2 PAD-OPEN 4x4m

+5VALWP 1 @P306 2 PAD-OPEN 4x4m

3.3VALWP
TDC 2.78A
Peak Current 3.972A
OCP current 4.726A

5VALWP
TDC 3.91A
Peak Current 5.585A
OCP current 6.647A

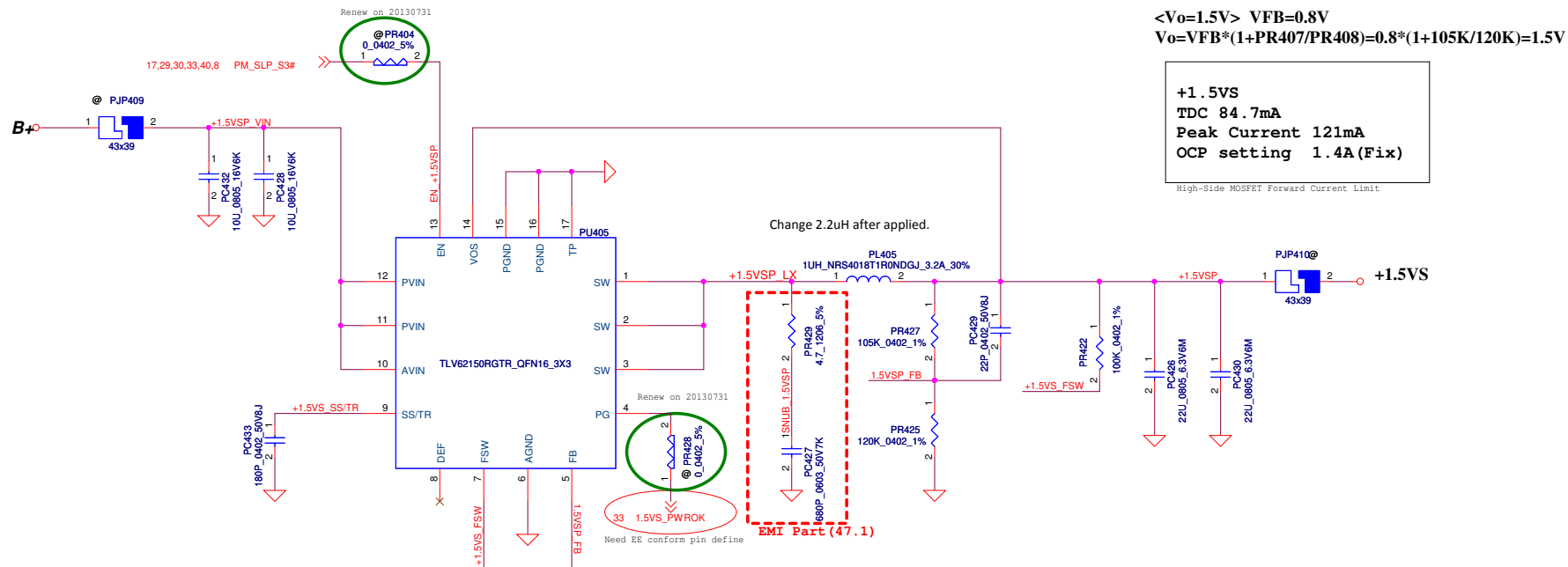
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/06/02		2013/10/28		P37-PWR +3.3/5V VR	
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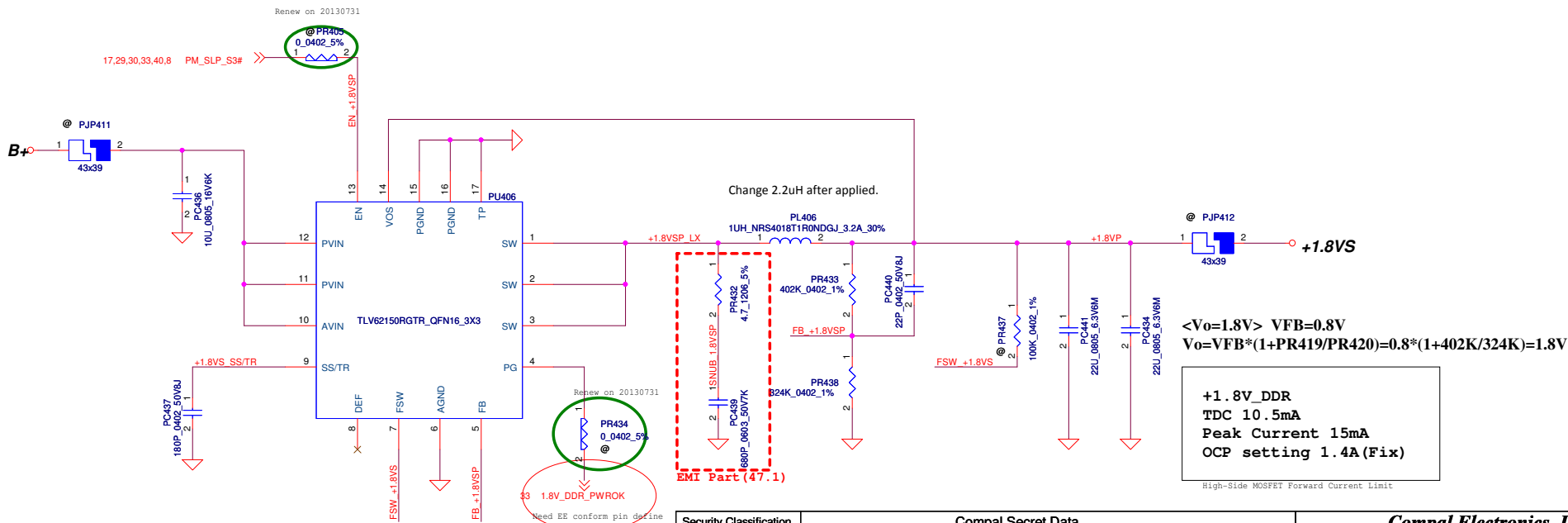
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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				Size	Document Number
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P39-PWR +3.3V_VR(2/2)
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				Date:	Wednesday, August 14, 2013
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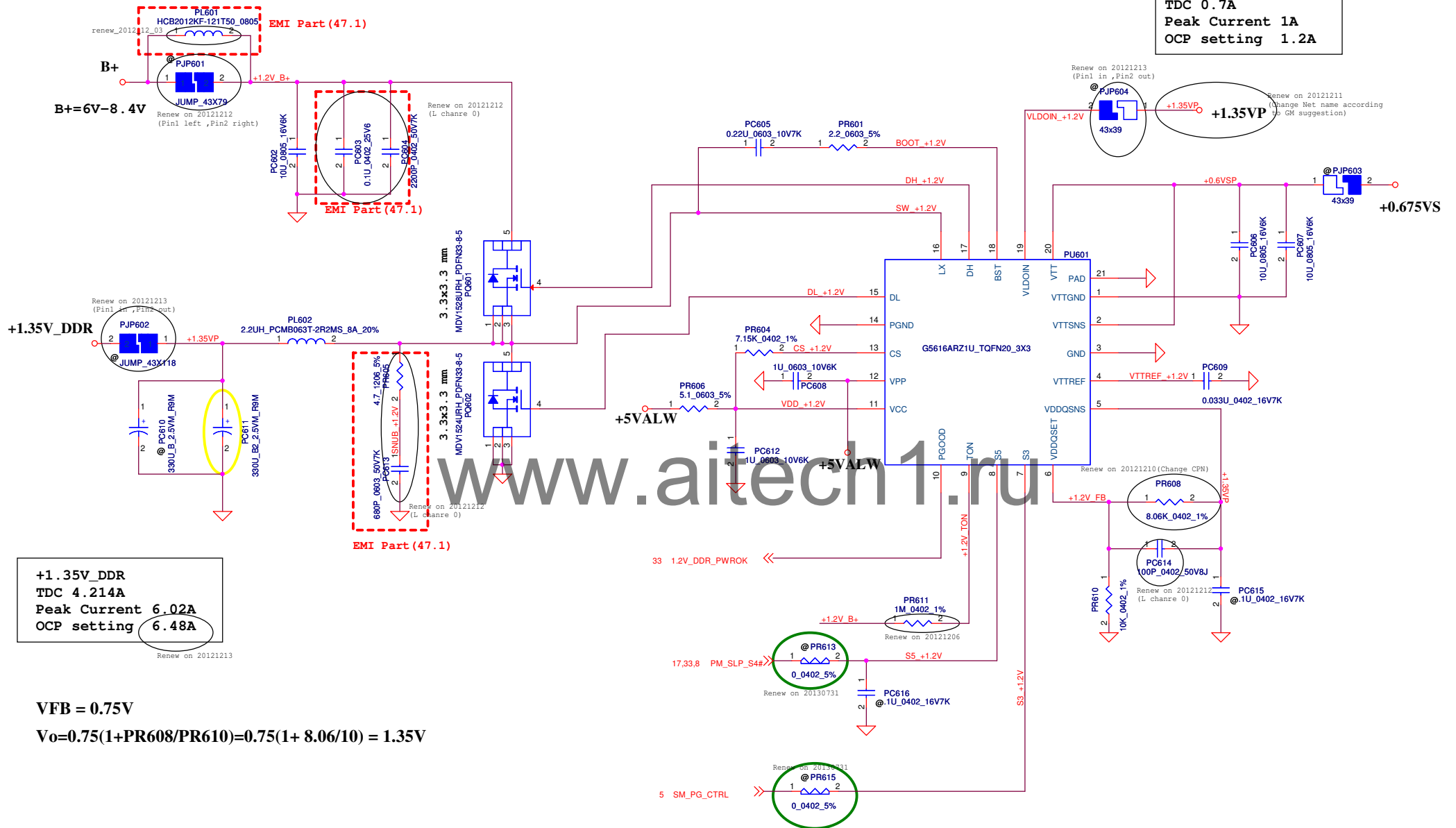
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						Size		Document Number		Rev	
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DDR controller(35.3), Support component(35.4)

```
+0.675VS
TDC 0.7A
Peak Current 1A
OCP setting 1.2A
```

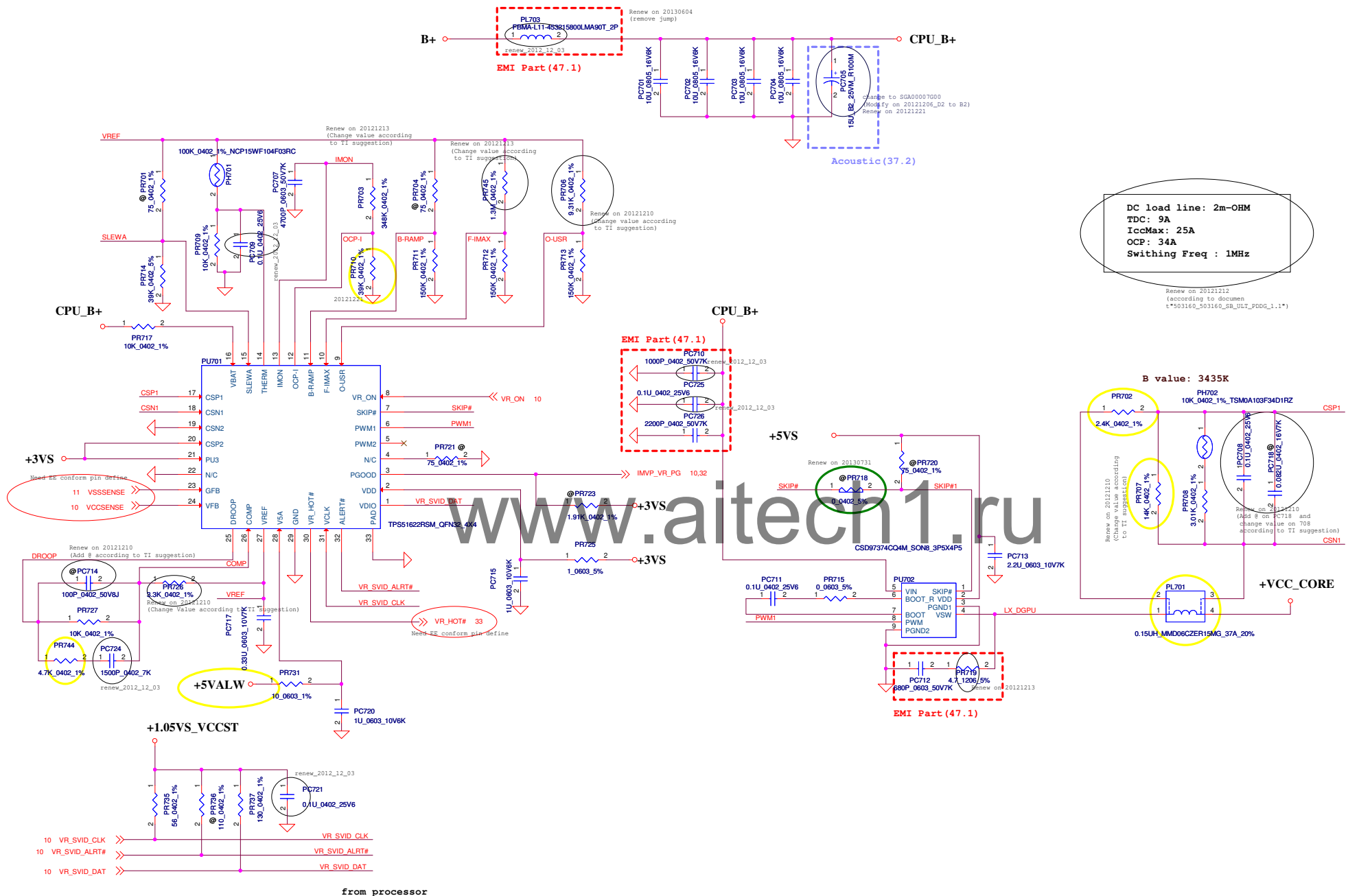


```
+1.35V_DDR
TDC 4.214A
Peak Current 6.02A
OCP setting 6.48A
```

$$V_{FB} = 0.75V$$

$$V_o = 0.75(1 + PR_{608}/PR_{610}) = 0.75(1 + 8.06/10) = 1.35V$$

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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title P42-PWR +1.2V DDR/+0.6VS		
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P43-PWR CPU CORE
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+VCC_CORE



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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P44-PWR PROCESSOR DECOUPLING	
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				Date:	Wednesday, August 14, 2013	Sheet 44 of 49

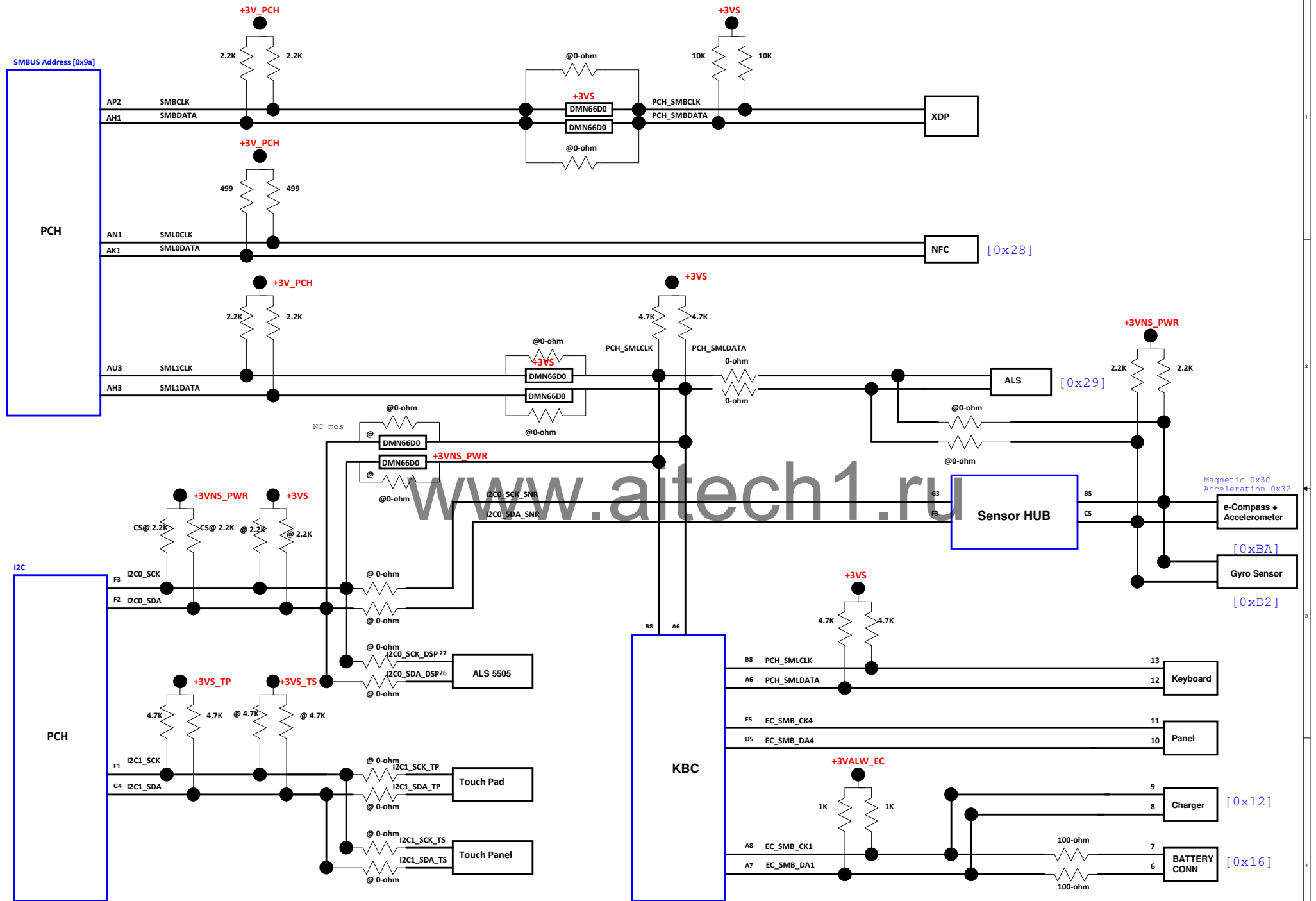
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Title		
P45-LED converter TP961101A		
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		A00
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.	
	36		20121008	Compal_Power	create one more input cap for TPS51362 Vin	add PC513_10U_0805_16V6K for TPS51362's input	
	34		20121012	Compal_HW	create one more resistor for TPS62130 enable pin	add PR342_2.2K_0402_5%	
	34		20121018	Compal_Power	design change, delete PU301~PU305, TPS62130 and related components, create PU301, TPS51225 for 3.3V and 5V power rails		
	35						
	36						
	36		20121018	Compal_Power	design change, delete PU401, PU402, TPS62140 and TPS62150 and related components, create PU401and PU402, SY8003D for 1.5V and 1.8V power rails		

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		2013/10/28		Title	
				P46-PWR PIR-1	
				Document Number	
				LA-A161P	
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				A00	
				Date	
				Wednesday, August 14, 2013	
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[AC in]

[Battery only, AC absent]

EC pay attention timing

Discrete Power On Sequence

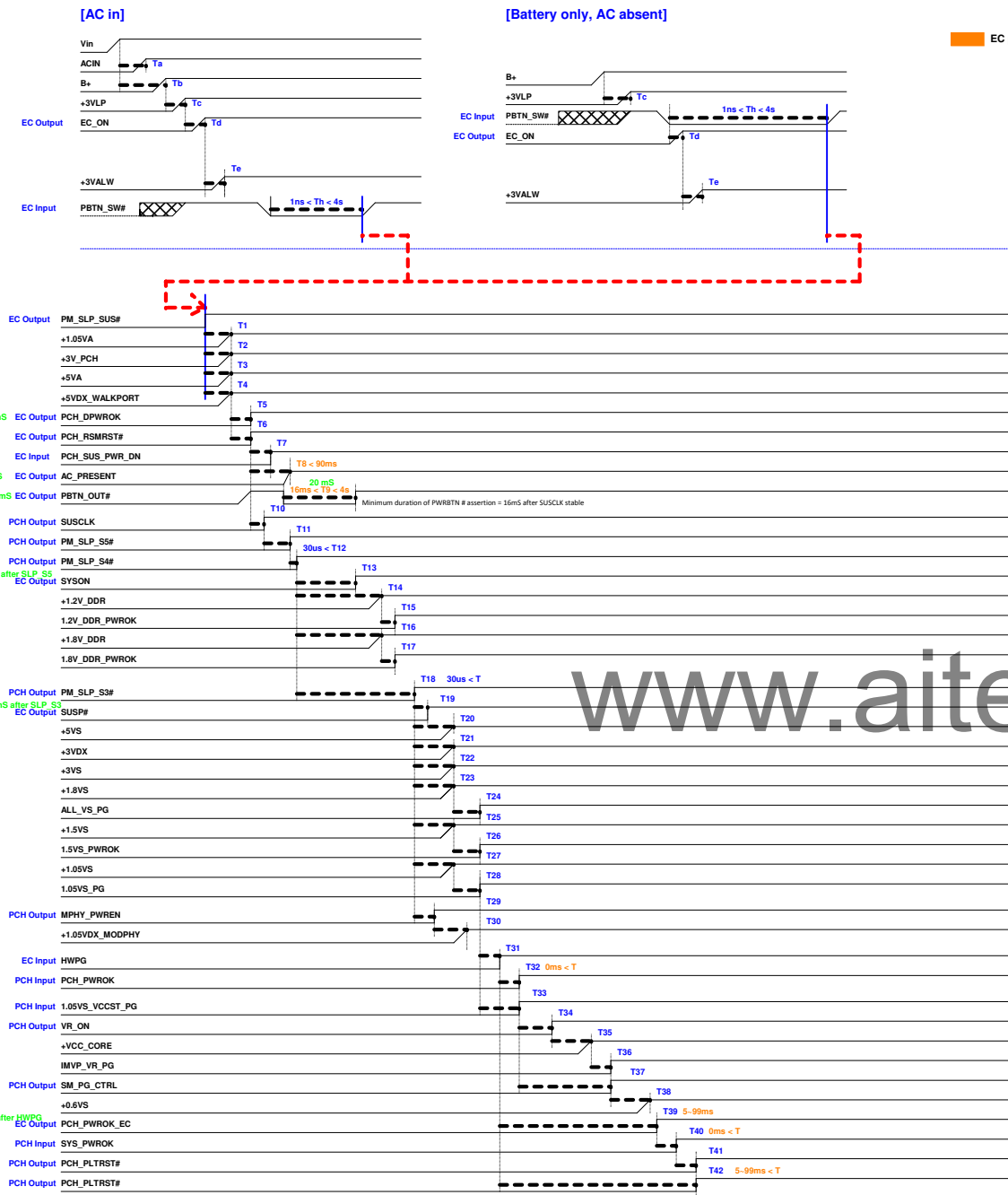
[AC in]

[Battery only, AC absent]

ITEM	Measure Point	Time
Ta	Vin	To
Tb	ACIN	To
Tc	B+	To
Td	+3VLP	To
Te	+3VALW	To
Tf	EC_ON	To
Tg	PBTN_SW#	To
Th	PBTN_SW#	Low pulse width

ITEM	Measure Point	Time
To	B+	To
To	+3VLP	To
To	PBTN_SW#	Low pulse width
To	EC_ON	To
To	+3VALW	To
To	EC_ON	To
To	PBTN_SW#	Low pulse width

ITEM	Measure Point	Time
T1	PM_SLP_SUS#	To
T2	PM_SLP_SUS#	To
T3	PM_SLP_SUS#	To
T4	PM_SLP_SUS#	To
T5	+3V_PCH	To
T6	+5V_PCH	To
T7	+5V_PCH	To
T8	+5V_PCH	To
T9	+5V_PCH	To
T10	+5V_PCH	To
T11	+5V_PCH	To
T12	+5V_PCH	To
T13	+5V_PCH	To
T14	+5V_PCH	To
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T39	+5V_PCH	To
T40	+5V_PCH	To
T41	+5V_PCH	To
T42	+5V_PCH	To



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